Energy Research and Development Division
FINAL PROJECT REPORT

DEVELOPMENT OF FAULT CURRENT CONTROLLER TECHNOLOGY

Prototyping, Laboratory Testing, and Field Demonstration

Appendices

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PREFACE

The California Energy Commission Energy Research and Development Division supports public interest energy research and development that will help improve the quality of life in California by bringing environmentally safe, affordable, and reliable energy services and products to the marketplace.

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- Transportation

Development of Fault Current Controller Technology is the final report for the Development of Fault Current Controller Technology project (contract number UC MR-064) conducted by University of California, Irvine. The information from this project contributes to Energy Research and Development Energy Systems Integration Program.

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ABSTRACT

Fault current controller technology, also frequently referred to as fault current limiter technology, has been identified as a potentially viable solution for expanding the capacity of the transmission system and its service life to meet the growing demand for electricity by addressing the impacts of the resulting higher fault currents. This report discusses the development and field demonstration of distribution-class fault current controller technology. The project focused on prototyping, test plan development, laboratory testing, and field testing and demonstration, with a view toward potential further technical development and application of the technology in transmission-level systems.

A full-size three-phase distribution-level high-temperature superconducting fault current controller prototype was designed, built, and field-tested. The prototype fault current controller went through several iterations of extensive testing prior to field installation. It was then installed for field demonstration from March 2009 through October 2010.

The research team completed an initial design for a fault current controller based on solid-state (power electronics) technology. Initial analysis indicated that design changes to the prototype were necessary to improve its thermal management, the immunity of the control circuits to noise and interference and to address mechanical issues. The additional cost for these items was beyond the scope and budget of this project so this prototype design did not advance to the laboratory and field test stages during the project period.

This report provided a survey of fault current controller technology development status, including both the saturable-core and solid-state types represented by this project, followed by detailed design considerations, laboratory test procedures and results, field test installation and metering, and field demonstration outcomes. The report concluded with a summary of the lessons learned and recommendations for future fault current controller research efforts and commercial industry applications.

Keywords: Fault Current, Fault Current Controller, FCC, Fault Current Limiter, FCL, Short Circuit Current, Power System Protection, Saturable-core Reactor FCL, Solid-State FCL, High Temperature Superconductivity, HTS

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APPENDIX A:
Zenergy Power HTS FCL Test Plan

Engineering Specifications

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Responsible Person:	Francisco De La Rosa				
Project Name:	High Temperature Superconductor Fault Current Limiter				
Document Title:	Test Protocol for FCL 15kV, 1.2kA, 3 Phase				
Document #:	**ZP/ES-2008-05**	Reg: #		Page 1	
Date of issue:	05/05/08	Classification:	Confidential	No. of pages:	33
Client(s):	Zenergy Power				
Author(s):	F. De La Rosa	Approved:	F. Moriconi	Order No.:	
Distribution:	Franco Moriconi, Bert Nelson, Woody Gibson, Robert Lombaerde, Amandeep Singh, William Schram, Frank Darmann				
Distribution page 1:					
Keywords:	Fault current limiter, high temperature superconducting, air-core reactors, discharge current-limiting reactors, dry-type air-core reactors, dry-type reactors, saturable reactors, filter reactors, reactors, series–connected reactors, series reactor applications, FCL reactor test				

Summary: General tests to apply to the Fault Current Limiter according to ZENERGY Power internal procedures for power current characterization and transient faults as well as recommended tests by IEEE relevant standard for Series Connected Reactors and dry-type transformers are described in this document.

Contents **Page**

1. Summary of Tests to be performed on FCL

a. "**Pre-connection Tests"** consisting on steady state and fault current characterization under nominal voltage and load current

b. Testing according to IEEE C57.16-1996 and IEEE C57.12.01-2005

These pertinent tests are summarized in table 1

#	TEST	Location	Ref.	Observations
1	Pre-connection	Powertech	8.1-8.2	
2	Winding Resistance	T&R	9.1	
3	Impedance	T&R	9.2	
4	Total loss	T&R	9.3	
5	Temperature rise	T&R	9.4	Must be carried out at rated current. Reduced voltage is allowed.
6	Applied voltage	T&R	9.5	@34kV according to coil manufacturer and IEEE C57.12.01
7	Radio influence voltage(RIV)	-	9.6	Not applicable for 15kV class
8	Turn-to-turn	Powertech	9.7	
9	Lightning impulse @110 kV	Powertech	9.8	
10	Chopped-wave impulse	Powertech	9.9	
11	Audible sound	T&R or Shandin	9.10	
12	Insulation power factor	T&R	11.3	
13	Insulation resistance	T&R	11.1	
14	Partial Discharge	T&R	11.2	

Table 1: ZENERGY FCL Test Summary

2. General

This report presents the test protocol for the ZENERGY Power High Temperature Superconductor Fault Current Limiter**.** The protocol is largely based on the IEEE C57.16-1996 and IEEE C57.12.01-2005 relevant standards. These address testing procedures for Dry-Type Series-Connected Reactors and Dry-type Distribution and Power Transformers including those with Solid Cast and/or Resin-Encapsulated Windings, respectively. These reactors are connected in the power systems to control power flow under steady state conditions and/or limit fault current under short circuit conditions.

The tests include Impedance measurements, total loss measurements, applied voltage, radio Influence voltage (RIV), turn-to-turn, lightning impulse, chopped-wave impulse test, audible noise, dielectric insulation, partial discharge and average sound level, among other tests.

3. Scope

The scope of this work is to portray the test procedures to which the ZENERGY Power HTS Fault Current Limiter shall be submitted previous to the ZENERGY Power short-circuit testing protocol.

4. Applicability

High temperature superconducting ZENERGY Power Fault Current Limiter.

5. Applicable documentation

- IEEE Std C57.16-1996, IEEE Standard Requirements, Terminology, and Test Code for Dry-Type Air-Core Series-Connected Reactors
- IEEE Std C57.12.01-2005, IEEE Standard General Requirements for Dry-Type Distribution and Power Transformers Including Those with Solid Cast and/or Resin-Encapsulated Windings
- NEMA -107-1987, Methods of Measurements of Radio Influence Voltage (RIV) of High Voltage Apparatus

6. Acronyms and definitions

6.1 Acronyms

FCL	Fault Current Limiter
HTS	High Temperature Superconductor
TBD	To Be Determined

6.2 Definitions

Current Limiting Reactor: A reactor connected in series with the phase conductors for limiting the current that can flow in a circuit under short circuit conditions, or under other operating conditions, such as capacitor switching, motor starting, synchronizing, arc stabilization, etc.

Rating of a Series Reactor: The current that a series reactor can carry at its specified reactance together with any other defining characteristics, such as system voltage, Basic Insulation Level (BIL), short circuit current (thermal and mechanical) duty, and frequency.

Rated current: The root mean square (rms) power frequency current in amperes that can be carried for the duty specified, at rated frequency without causing further measurable increase in temperature rise under prescribed conditions of test, and within limitations of established standards.

Short time duty: A requirement of service that requires operation at substantially constant current for a short and definitely specified time.

Nominal voltage: A line to line voltage assigned to a system or circuit of a given voltage class for the purpose of convenient designation.

Rated system voltage: The voltage of a series reactor to which operational and performance characteristics are referred. It corresponds to the nominal line-to-line or phase-to-phase system voltage of the circuit in which the reactor is intended to be used.

Effective resistance (or ac resistance): The value of resistance of a series reactor obtained by dividing the total losses by the current squared at power frequency.

Losses: Those losses are due to current flow. They include:

- The resistance and the eddy-current loss in the winding due to load current
- Losses caused by circulating current in parallel windings
- Stray losses caused by magnetic flux in other metallic parts of the reactor support structure, and in the reactor enclosure when the support structure and the enclosure are supplied as an integral part of the reactor insulation.

Impedance: The phasor sum of the reactance and resistance, expressed in ohms.

Impedance voltage drop: The product of the rated ohms' impedance and the rated current of a series reactor.

Per unit reactance: On a rated current base, a dimensionless quantity obtained by referencing the magnitude of the reactance to the rated system line-to-neutral voltage divided by the rated current of the reactor. It can also be defined on an arbitrary megavoltampere (MVA) base.

Rated inductance: The total installed inductance at a specified frequency. It may consist of mutual as well as self inductance components.

Rated reactance: The product of a rated inductance and rated angular frequency that provides the required reduction in fault current or other desired modification to power circuit characteristics.

Reactance: The product of the inductance in henries and the angular frequency of the system.

Reactance voltage drop: The component of voltage drop in quadrature with the current.

Resistance voltage drop: the component of voltage drop in phase with the current.

Ambient sound-pressure level: Is the sound-pressure level measured in the test facility without the reactor energized.

Sound-Pressure level, in decibels: is 20 times the logarithm to the base 10 of the ratio of the measured sound pressure to a reference pressure of 20 Pa.

Sound-Power level, in decibels: is 10 times the logarithm to the base 10 of the ratio of the emitted sound power to a reference power of 10-12 W.

Semireverberant facility: is a room with a solid floor and an undetermined amount of sound-absorbing materials on the walls and ceiling.

7. Service Conditions

7.1 Ambient temperature

This is the temperature of the air surrounding the reactor. For the purposes of IEEE Std C57.16-1996, it is assumed that the temperature of the cooling air (ambient temperature) does not exceed 40 ^{o} C and the average temperature of the cooling air for any 24 hour period does not exceed 30 ^{o} C.

7.2 Environmental and application related service conditions

Reactor for outdoor application must be designed for conditions such as rain, (ice), snow, fog and ultraviolet (UV) ray exposure. The purchaser should attempt to quantify or qualify environmental conditions, including type and level of pollution. The reactor should also be designed to withstand, without damage or loss of service life, mechanical loads such as electromagnetic forces during short-circuit, wind loading, and stresses caused by thermal expansion and contraction due to ambient temperature and current loading variations. Wind speed data, including gust factors, should be specified by the purchaser.

8. ZENERGY Pre-Connection Tests

ZENERGY shall apply a number of pre-connection tests including steady state (applied voltage and load current) and Fault Current Characterization, as depicted in tables 2 and 3.

8.1 Steady state test

Secondary Voltage of main transformer bank	Steady state current through FCL required	Load bank impedance on load side of FCL	Source limiting impedance	Time duration of steady state current	Cooling time
kV	A	Ω	Ω	s	min
13.1	200	TBD	As required	100	<20
13.1	500	TBD	As required	100	<20
13.1	750	TBD	As required	100	<20
13.1	1200	TBD	As required	100 max	20

Quantities to measure:

- Line current in the three phases
- Voltage drop across the FCL
- AC Coil temperature

Quantities to derive from measurements:

- FCL impedance
- Harmonics

Table 2: ZENERGY Pre-Connection Tests

8.2 Fault Current Characterization and Transient

FCL Status in circuit	Secondary voltage of main transformer (line to line)	Steady state line current before fault introduced	Load bank impedance required	Time duration of steady state current required	Steady state fault current on load side	Source limiting impedance required (nominal)	X/R	Time required for fault current to flow	Time required for steady state current to flow after fault
	kVrms	A(rms)	Ω	Cycles	kA (rms)	mΩ		cycles	cycles
Out/in	13.1	1200	17Δ	10	5	As needed	10-20**	30	20
Out/in	13.1	1200	17Δ	10	10	As needed	10-20**	30	20
Out/in	13.1	1200	17Δ	10	15	As needed	10-20**	30	20
Out/in	13.1	1200	17Δ	10	20*	As needed	TBD ***	TBD ****	20

- 3-phase fault. Single or 3 phase Point On Wave is possible
- 25 kA breaker available, but limited to 20 kA based on source side resistors when tested at Powertech
- ** Unmodified X/R of our source i.e. without addition of series resistors is approximately 40
- ***X/R must be adjusted in order not to exceed 20 kA symmetric fault
- ****Must not exceed thermal rating (will have to be <than 30 cycles)

Table 3. ZENERGY Pre-Connection Tests

9. Testing Plan according to IEEE C57.16-1996

- The recommended tests adapted from this relevant standard are described in tables 4 through 5 below.

Test	When performed	Test classification		
		Routine	Design	Other
Resistance measurement	The dc resistance measurement shall be made on all units.	X		
Impedance measurement	The impedance measurement shall be made on all units.	X		
Total loss measurement	Total losses should be measured on all counts.	X		
Temperature rise test	This test is performed on one unit out of a number of units of the same design.		X	
Applied voltage test	The applied voltage test shall be made only on support insulators when specified.			X
Radio influence voltage (RIV) test	This test is performed for nominal system voltages 230 kV and above only when specified.			X
Turn-to-Turn test	This test is performed for nominal system voltages of 34.5 kV and below.	X		
Lightning impulse test —Nominal system voltage greater than 34.5 kV —Nominal system voltage at or below 34.5 kV	The lightning impulse test should be performed on all units. The lightning impulse test should be performed only when specified.	X		X
Switching impulse test	The switching surge test shall be made on the support structure (insulators) of series reactors rated 115 kV or above only when specified.			X
Chopped-Wave impulse test	The chopped-wave impulse test shall be made on series reactors only when specified.			X
Audible sound test	Units shall be tested only when specified.			X
Seismic verification test	The seismic verification test shall be made on series reactors only when specified.			X
Short-Circuit test			X	

Table 4: Routine, design and other test for dry-type series reactors

Routine tests
A routine test is a test made on each and every unit of a specific design and is primarily a verification of quality.
Routine tests shall be made on all series reactors in accordance with the requirements of Table 4.

Design tests
A design test (also referred to as a type test) is a test carried out on a single unit of a specific design and is primarily a verification of the ability to meet in-service application requirements. Design tests shall be made in accordance with the requirements of Table 4.

Other tests
A test designated as “other” is a test performed on one or all units of a specific design if requested by the purchaser. It is usually requested to demonstrate conformance to special application requirements as opposed to the more general application requirements covered by design tests. When specified (as individual tests), “other” special tests, as listed in Table 4, shall be made on series reactors.

For the Zenergy Power FCL 15kV class we shall apply the following tests:

- Resistance measurements
- Impedance measurements
- Total loss measurements
- Applied voltage test
- Turn-to-turn test
- Lightning impulse test
- Chopped-wave impulse test
- Audible sound test

and only if required by customer

- Radio Influence Voltage (RIV) test

9.1 Resistance measurements

Resistance measurements are of fundamental importance for three purposes:
a) For the calculation of the conductor I^2R loss.
b) For the calculation of winding temperatures at the end of a temperature rise test.
c) For a quality check among units of the same rating.

Cold winding resistance measurements are normally converted to a standard reference temperature equal to the rated average winding temperature rise plus 20 °C. In addition, it may be necessary to convert the resistance measurements to the temperature at which the impedance and loss measurements were made. The conversions are accomplished by the following formula:

$$R_s = R_m \frac{(\theta_s + \theta_k)}{(\theta_m + T_k)} \qquad (1)$$

where
R_s is the resistance at the desired temperature Θs
R_m is the measured resistance at temperature Θm
Θ_s is the desired reference temperature, in degrees Celsius
Θ_m is temperature at which resistance was measured, in degrees Celsius, and
Tk is 234.5 (Copper) and 225 (Aluminum)

Cold resistance measurements shall not be taken in less than 4 hours after the reactor has been moved from a location where ambient temperature differs by more that 5 ^{o}C, but less than 10 ^{o}C.

9.2 Impedance measurements

Resistance and reactance components of the impedance voltage are determined by the use of the following equations:

$$E_r = \frac{P_z}{I} \qquad (2)$$

$$E_x = \sqrt{E_z^{\ 2} - E_r^{\ 2}} \qquad (3)$$

where
Er is the resistive voltage,
Ex is the reactance voltage, quadratic component,
Ez is the impedance voltage of winding carrying current,
Pz is the watts quantity measured in the impedance test of winding carrying current, and
I is the current in amperes on that winding where the voltage is applied.

9.3 Loss measurements

Since many series reactors (especially high kilovoltampere units) operate at low power factors, small variations in frequency, deviations from the true sine wave in applied voltage, errors in measuring components, and electromagnetic interference may introduce significant errors in loss measurements. Proper test conditions and precision components specifically designed for low power factor measurements, are essential for an accurate determination of reactor losses.

a) Impedance bridges are frequently used to measure losses and are generally more accurate than traditional wattmeter measurements. While many configurations of impedance bridge networks are possible, the choice of a particular network shall be determined by the measurement problem at hand and the testing facilities available. It should be noted that modern electronic-based wattmeters can be highly accurate.

b) If wattmeters are used to measure losses, connections to the reactor will be the same as those shown in Figures 1 and 2. The voltage is adjusted to the desired value at rated frequency, and simultaneous readings of amperes, volts, watts, and frequency are taken. For low power factors, corrections shall be considered for phase angle and losses in the instruments and instrument transformers.

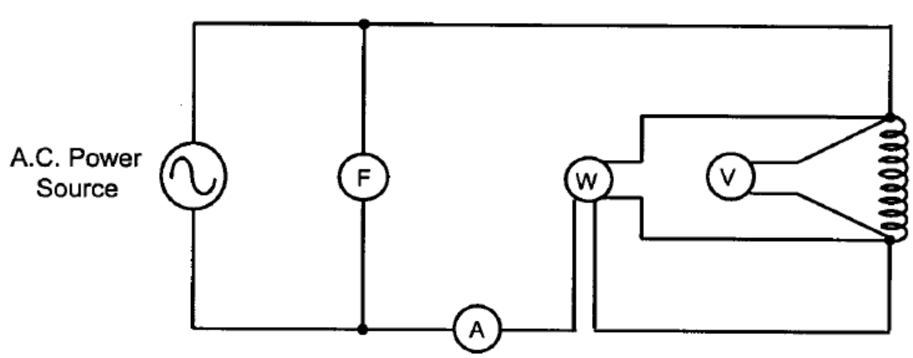


Fig.1: Single-Phase reactor connections for impedance-loss and impedance-voltage tests (instrument transformers to be added when necessary)

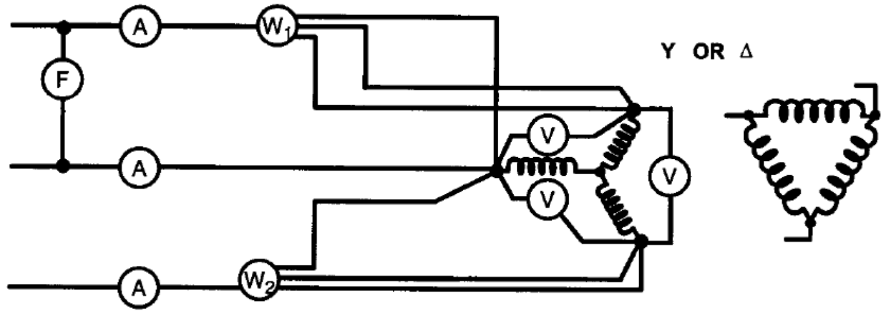


Fig. 2: Three phase reactor connections for impedance-loss and impedance-voltage tests (instrument transformers to be added when necessary)

9.3.1 Loss tests on dry-type series reactors

In these reactors, the losses consist of the I^2R (dc resistance) losses in the conductor, the eddy losses in the conductor, and any metallic framework of the clamping structure.

Since the losses in these reactors are proportional to I^2, the losses can be measured at 100% voltage, or at a reduced voltage. In either case, precision of measurement shall be demonstrated to the purchaser's satisfaction. The losses are to be corrected to rated current and a reference temperature. In some cases, the actual average winding rise as determined by the temperature rise test plus 20 °C may be used, which is an attempt to reflect actual in-service losses and actual site average ambient temperature.

9.3.2 Temperature of the winding

The temperature of the winding shall be taken immediately before and after the impedance measurements in a manner similar to that described for resistance measurements above. The average shall be taken as the true temperature.

I^2R loss of the winding. The I^2R loss of the winding is calculated from the ohmic resistance measurements (corrected to the temperature at which the impedance test was made) and the currents that were used in the impedance measurement. These I^2R losses subtracted from the impedance watts give the stray losses of the winding. When reactor windings are enclosed in shielded housings or tanks, part or all of which are magnetic material, part of the stray loss must be considered with the winding I^2R when correcting losses from measured temperature to other temperatures. Since this varies with the proportions of the reactor design and type of shield, it will have to be approximated for each design but can be checked by measurement of loss at the start and finish of the temperature run.

9.3.3 Per-Unit values

Per-Unit values of the resistance, reactance, and impedance voltage are obtained by dividing the corresponding voltages by the rated voltage. Percentage values are obtained by multiplying per-unit values by 100.

9.3.4 Impedance-Loss and impedance-voltage test of a three-phase reactor

Balanced three-phase voltages of rated frequency and suitable magnitude are applied to the terminals to force rated current to circulate (see Figure 2).

9.3.5 Procedure

The procedure is similar to that described for single-phase units, except that all connection and measurements are three phase instead of single phase.

9.3.6 Line currents

If the three line currents cannot be balanced, their average rms values should correspond to the desired value.

9.3.7 Stray-Loss component

The stray-loss component of the impedance watts is obtained by subtracting from the latter the I^2R losses of the reactor.

9.3.8 Temperature correction

Temperature correction shall be made as described above.

9.3.9 Bridge method

Bridge methods are preferred as they are generally more accurate than the wattmeter method. However, it should be noted that modern electronic-based wattmeters can be highly accurate.

9.3.10 Temperature correction for losses

The I^2R component of the impedance loss increases with the temperature, the stray-loss component diminishes with the temperature, and therefore, when it is desired to convert the impedance losses from one temperature to another, the two components of the impedance loss are converted separately.

Thus,

$$P_r = P'_r \frac{T_k + \theta}{T_k + \theta'} \qquad \text{-------------------} \qquad (4)$$

$$P_s = P'_s \frac{T_k + \theta'}{T_k + \theta} \quad P_r = P'_r \frac{T_k + \theta}{T_k + \theta'} \qquad \text{-------------------} \qquad (5)$$

where

Tk is 234.5 for copper, and
Tk is 225 for aluminum

Pr and *Ps* are I^2R and stray losses, respectively, at the specified temperature q. *P´r* and *P´s* are measured I^2R and stray losses at temperature q´. q and q´ are in degrees Celsius.

9.4 Temperature Rise

9.4.1 Loading conditions.

Temperature rise test shall be done under load conditions that impose losses as close as possible to those obtained at rated frequency with rated current in the windings. If laboratory power is not sufficient or power control adjustment is not enough to carry out a test at rated current, testing at current levels down to 90% of rated is permissible. In the case of reactors to be installed in a side-by-side configuration, testing of single unit is representative. In case of reactors mounted in three phase configuration, they should be tested in the installed configuration with a three-phase current supply unless otherwise agreed upon between purchaser and manufacturer. Reactors should be completely assembled. The ambient temperature shall be taken as that of the surrounding air, which should be preferably not less than 10 ^{o} C, not more than 40 ^{o} C.

9.4.2 Temperature rise – General.

Temperature rise of metal parts, other than the winding conductor in contact with, or adjacent to insulation, or of other metal parts, shall be determined by thermocouple or by thermometer when required. Caution should be taken with the use of thermocouples to measure surface temperature due to parts being at high voltage. The temperature rise of the winding should be determined by the resistance method, or by a thermometer when so specified. The test current shall be adjusted to produce the total fundamental plus harmonic winding losses as described in Annex A in the IEEE Std C57.16-1996. Also, aspects related to minimization of errors temperature rise of metal parts should be taken into consideration as described in the cited standard.

The **ultimate temperature rise** is considered to be reached when the temperature rise becomes constant. i.e., when temperatures measured by thermometers or thermocouples on the winding do not vary more than 2.5% or 1^{o} C, whichever is greater, during a period of two consecutive hours and the duration of the heat run is at least five thermal time constants.

9.4.3 Altitude effects

When a reactor that is tested at an altitude less than 1000 m (3300 ft) is to be operated at an altitude in excess of 1000 m, it shall be assumed that the observed temperature rise will increase in accordance with the following relation:

Increase in temperature rise at altitude A m(ft) =

$$(Temp\_increase@Altitude\_A\_m[ft]) = (Observed\_rise)\left(\frac{A}{A_0} - 1\right)F \quad \text{- -} \quad (6)$$

where

A_0 is 1000 m (3300 ft), and

F is an empirical factor equal to 0.05.

NOTE — The “observed rise” in the foregoing equation is winding rise over the ambient temperature.

9.4.4 Temperature effects

When the ambient air temperature is other than 30 °C, a correction shall be applied to the temperature rise of the winding by multiplying it by the correction factor C, which is given by the ratio

$$C = \frac{T_k + 30}{T_k + \theta} \text{- - - - - - - - - - - - - - - - - - -} \quad (7)$$

where

Tk is 234.5 for copper,

Tk is 225 for aluminum, and

θ is the ambient air temperature, in degrees Celsius

9.5 Applied Voltage

An applied voltage test shall be made on the reactor’s supporting structure, including insulators. For this FCL unit that uses cast resin coils the test value for the applied voltage test is 34 kV.

9.6 Radio influence voltage (RIV) test

According to IEEE STD. C57.16, RIV test is only required for series reactors operating at system voltages 230 kV and higher and is carried out at power frequency according to NEMA 107-1987.

9.7 Turn-to-turn overvoltage test

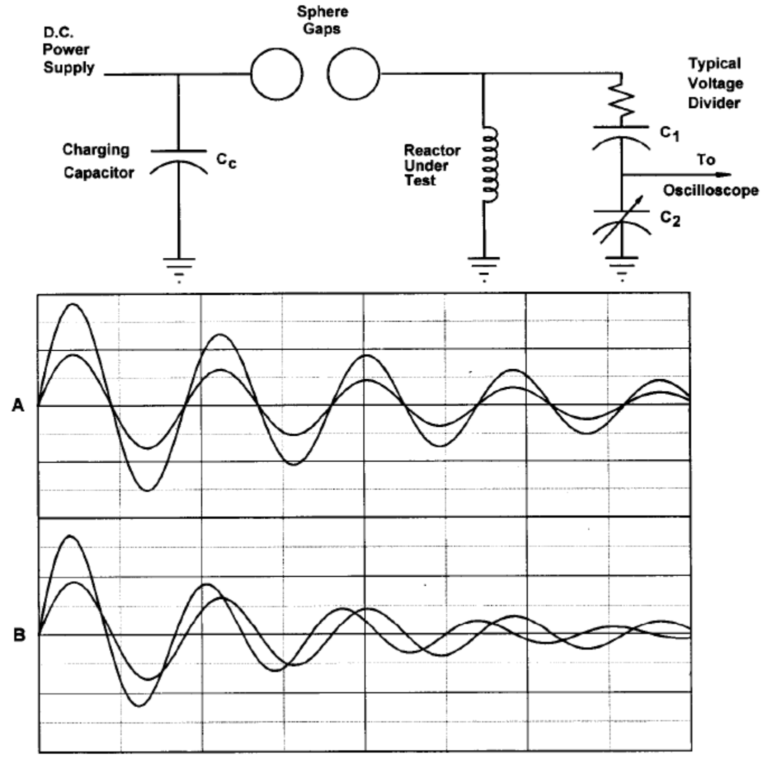
The turn-to-turn test shall consist of a series of high frequency, exponentially decaying exponential voltages between the terminals of each winding, as per IEEE Std C57.16-1996 application procedure.

The turn-to-turn test is performed by repeatedly charging a capacitor and discharging it, through sphere gaps, into the reactor windings. The type of overvoltage that the reactor is subjected to is more representative of a switching overvoltage, with an exponentially decaying sinusoidal waveshape. The test duration is for 1 min and the initial crest value of each discharge is to be $\sqrt{2}$ times the rms value as specified in Table 5. The ringing frequency is a function of the coil inductance and charging capacitor, and is typically on the order of 100 kHz. The test shall consist of not less than 7200 overvoltages of the required magnitude.

Primary verification of winding insulation integrity should be based on oscillographic methods. A surge oscilloscope and camera are used to record the last discharge superimposed on a reduced voltage discharge. A change in period or rate of envelope decay, between the reduced and full waves, would indicate a change in coil impedance and thus an inter-turn failure. The crest test voltage level is $\sqrt{2}$ times the rms voltages listed in column 3 or 4 of Table 5.

Secondary verification of insulation integrity is by observation. A failure can be detected by noise, smoke, or spark discharge in the reactor windings.

Figure 3 shows the schematic of the test circuit and representative oscillograms of applied test voltage. The use of oscillograms for failure detection is based on change in ringing frequency and a change in rate of envelope decay (damping).



A: Oscillogram showing a reactor that passed the turn-to-turn test.
B: Oscillogram showing a reactor of the same rating as in Oscillogram A, but having a turn-to-turn fault.
ƒ Note the shift in frequency and the increased damping.

Fig. 3 – Recommended circuit for turn-to-turn testing

9.8 Impulse testing

For dry-type air-core series reactors with nominal system voltages greater than 34.5 kV unless otherwise specified, a lightning impulse test shall be made on each terminal of the reactor (one at a time) by applying a reduced wave and tree full waves, all of positive polarity with crest voltage in accordance with the assigned BIL as specified in table 5 subject to a tolerance of ±3%. Impulse testing is performed using a standard waveform that reaches peak value in 1.2 μs and decreases to half value in 50 μs. The tolerance on time to crest should normally be ±30%.

For convenience in measurement, the time to crest may be considered as 1.67 times the time interval measured on the front of the wave from 30% to 90% of the crest value. The tolerance on time to one-half of crest shall normally be ±20%. However, as a practical matter,

a) The time to crest shall not exceed 2.5 ms except for windings of large impulse capacitance (low-voltage, high kVA and some high-voltage, high kVA windings).

To demonstrate that the large capacitance of the winding causes the long front, the impulse generator series resistance may be reduced, which should cause superimposed oscillations. Only the inherent generator and lead inductances should be in the circuit.

b) The impedance of some windings may be so low that the desired time to the 50% voltage point on the tail of the wave cannot be obtained with available equipment. In such cases, the manufacturer should advise the purchaser at proposal stage of the wave shape limitation. Based on agreement, waves of shorter duration are acceptable.

The virtual time zero can be determined by locating points on the front of the wave at which the voltage is, respectively, 30% and 90% of the crest value and then drawing a straight line through these points. The intersection of this line with the time axis (zero-voltage line) is the virtual time zero.

If there are oscillations on the front of the waves, the 30% and 90% points shall be determined from the average, smooth wave front sketched in through the oscillations. The magnitude of the oscillations preferably should not exceed 10% of the applied voltage.

When there are high-frequency oscillations on the crest of the wave, the crest value shall be determined from a smooth wave sketched through the oscillations. If the period of these oscillations is 2 µs or more, the actual crest value shall be used.

9.8.1 Reduced full-wave test

This wave is the same as a full wave except that the crest value shall be between 50% and 70% of the full-wave value given in Table 5.

9.9 Chopped-Wave test

When specified, this wave shall be the same as a full wave except that the crest value shall be at the required higher level given in Table 5 and the voltage wave shall be chopped at or after the required minimum time to sparkover. In general, the gap or other equivalent chopping device shall be located as close as possible to the terminals and the impedance shall be limited to that of the necessary leads to the gap; however, it shall be permissible for the manufacturer to add resistance to limit the amount of overswing to the opposite polarity to 50% of the amplitude of the chopped wave. The value of resistance added should not increase the time to chop of the chopped wave.

Impulse tests are generally applied in the following order: one reduced full wave, one full wave, one reduced chopped wave, two chopped waves, and two full waves (preferably within 10 minutes about the last chopped wave).

9.9.1 Wave polarity

For dry-type series reactors, the test wave shall be positive polarity unless otherwise specified.

9.9.2 Wave-Shape control

The maximum half value time t_2 of an impulse wave tail can be derived from the resonance frequency of the impulse generator capacitance (Cg) with the test object reactance (L_t).

$$t_2 = \frac{\pi}{3}\sqrt{L_t C_g} \quad \text{-------------------} \quad (8)$$

This is a theoretical value applying to an undamped oscillation with an opposite polarity peak of 100%. Various amounts of circuit damping will reduce this value accordingly. For instance, with a limitation of 50% for the opposite polarity peak, t_2 is

$$t_2 \approx \sqrt{0.5 L_t C_g} \quad \text{-------------------} \quad (9)$$

Equations (8) and (9) are based on the standard impulse test circuit. Values of t_2 < 50 µs are typical for low inductance reactors. Values of t_2 close to or exceeding those calculated using equations (8) and (9) can be achieved with the use of an inductor in parallel with the series (front) resistor of the impulse circuit with compromises generally required between wave duration, opposite polarity peak, wave front time, and peak overshoot.

The manufacturer may also elect to test a low-impedance winding by inserting a resistor of not more than 500 W in the grounded end of the winding. Although this will improve the impulse wave shape, the largest portion of the test voltage will be across the resistor and not across the test coil windings. Therefore, a shorter impulse wave tail is preferable to the insertion of a series resistor between the test object and ground.

9.9.3 Impulse oscillograms

All impulses applied to a reactor shall be recorded by a cathode-ray oscillograph or by suitable digital transient recorder. These oscillograms shall include voltage and ground-current oscillograms for *all* full-wave and reduced full-wave impulses. Sweep times should be on the order of 2 µs to 5 µs for chopped-wave tests, 50 µs to 100 µs for full-wave tests, and 100 µs to 600 µs for ground-current measurements.

All voltage and current oscillograms should be included in the test report, including all relevant calibration shots.

9.9.4 Connections for impulse tests

In general, the tests shall be applied to each terminal one at a time.

9.9.5 Terminals not being tested

One terminal of the winding under test shall be grounded through a low-resistance shunt so that ground current measurements can be made. The resistance of the current shunt should typically be less than 0.1% of the reactance of the test object (reactor) at 5 kHz. The 5 kHz reference frequency is based on the half period of a standard lightning impulse being on the order of 100 µs.

9.9.6 Detection of failure during impulse test

Because of the nature of impulse test failures, one of the most important matters is the detection of such failures. There are a number of indications of insulation failure.

9.9.7 Ground current oscillograms

In this method of failure detection, the impulse current in the grounded end of the winding tested is measured by means of a cathode-ray oscillograph or by suitable digital transient recorder connected across a suitable shunt inserted between the grounded end of the winding and ground. Any differences in the wave shape between the reduced full wave and final full wave detected by comparison of the two current oscillograms may be indications of failure or deviations due to non injurious causes. A complete investigation is required and should include an evaluation by means of a new reduced-wave and full-wave test. Examples of probable causes of different wave shapes are operation of protective devices or conditions in the test circuit external to the series reactor.

The ground current method of detection is not suitable for use with chopped-wave tests.

It is difficult to shield the measuring circuit completely from the influence of the high voltage of the surge generator, and some stray potentials are frequently picked up that may produce an erratic record for the first 1 µs or 2 µs. Such influences, if they occur at the start of the current wave (and, to a lesser extent, at the start of the voltage wave), should be disregarded.

Where the impedance of the series reactor tested is high with respect to its series capacitance, current measurements may be difficult to make because of the small impulse current. In order to reduce the initial large capacitance current and maintain a reasonable amplitude for the remainder of the wave, a capacitor may be included in the current measuring circuit. The capacitor should not be larger than required to achieve this result.

9.9.8 Voltage oscillograms

Any unexplained differences between the reduced full wave and final full wave detected by comparison of the two voltage oscillograms, or any such differences observed by comparing the chopped waves to each other and to the full-wave up to the time of flashover, are indications of failure. Deviations may be caused by conditions in the test circuit external to the series reactor and should be fully investigated and confirmed by a new reduced-wave and full-wave test.

Other techniques that can be employed to investigate a suspected problem during the impulse test are the application of additional reduced waves and the subsequent comparison of these oscillograms with the original, the application of a series of full-wave impulses and an examination of the oscillograms for evidence of progressive change and, if a digitally based test system is being employed, the transfer function can be utilized.

Nominal system voltage (kV)	Applied voltage test (kV) rms	Turn-to-Turn overvoltage Indoor (kV) rms	Turn-to-Turn overvoltage Outdoor (kV) rms	BIL and full wave (kV) crest	Chopped-Wave (kV) crest	Time to flashover (µs)	Switching impulse (kV) crest
Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8
1.2	10	10	13	45	50	1.25	—
2.5	19	19	25	60	66	1.5	—
5.0	26	26	35	75	83	1.6	—
8.7	36	36	48	95	105	1.8	—
15.0	50	50	67	110	120	2.0	—
25.0	70	70	93	150	165	3.0	—
34.5	95	95	127	200	220	3.0	—
46.0	120	—	—	250	275	3.0	—
69.0	120	—	—	250	275	3.0	—
	175	—	—	350	385	3.0	—
115.0	175	—	—	350	385	3.0	280
	—	—	—	450	495	3.0	375
	280	—	—	550	605	3.0	460
138.0	—	—	—	450	495	3.0	375
	280	—	—	550	605	3.0	460
	335	—	—	650	715	3.0	540
161.0	280	—	—	550	605	3.0	460
	335	—	—	650	715	3.0	540
	385	—	—	750	825	3.0	620
230.0	335	—	—	650	715	3.0	540
	385	—	—	750	825	3.0	620
	—	—	—	825	905	3.0	685
	465	—	—	900	990	3.0	745
	545	—	—	1050	1155	3.0	870

Table 5: Insulation test levels for dry-type air-core series reactors

Nominal system voltage (kV)	Applied voltage test (kV) rms	Turn-to-Turn overvoltage Indoor (kV) rms	Turn-to-Turn overvoltage Outdoor (kV) rms	BIL and full wave (kV) crest	Chopped-Wave (kV) crest	Time to flashover (µs)	Switching impulse (kV) crest
Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8
345.0	465	—	—	900	990	3.0	745
	545	—	—	1050	1155	3.0	870
	—	—	—	1175	1290	3.0	975
500.0	610	—	—	1300	1430	3.0	1080
	680	—	—	1425	1550	3.0	1180
	710	—	—	1550	1705	3.0	1290
	—	—	—	1675	1845	3.0	1390
765.0	810	—	—	1800	1980	3.0	1500
	—	—	—	1925	2120	3.0	1600
	940	—	—	2050	2255	3.0	1700

NOTES:

1 — The nominal system voltage values given above are used merely as reference numbers and do not necessarily imply a relation to operating voltages.

2 — The applied voltage test on dry-type air-core series reactors is a high-voltage test on the insulators.

3 — For some BIL levels associated with a particular system voltage, no low-frequency test voltage is specified as insulators are not manufactured to that BIL rating.

4 — For system voltages greater than 34.5 kV, the turn-to-turn test is not applicable and a full-wave impulse test is to be performed as a routine test.

5 — In the case of series reactors, the BIL across the coil may be different than the BIL across the support insulators (to ground). The purchaser shall specify if the BIL across the coil is to be at a reduced level. Such a decision will be based on factors such as knowledge of the system characteristics and protection practices. Reduced BIL levels shall be selected from the standard values in Table 5.

6 — In the case of dry-type air-core series reactors, switching impulse insulation levels apply only to the support insulators for 115 kV system voltages and above.

7 — In the case of dry-type air-core series reactors employed in a three-phase stack configuration, interphase insulators may have a higher BIL rating than those at the base of the stack that only provide phase-to-ground insulation.

Table 5. Insulation test levels for dry-type air-core series reactors (Continued)

9.10 Audible sound-level test

The measurement of sound level on dry-type series reactors is an optional test. If such a test is to be performed, it should be carried out as far as applicable as described in IEEE Std C57.12.90-1993. Audible sound from dry-type air-core reactors originates principally in the reactor winding from which it is radiated as airborne sound. The frequency spectrum of the audible sound for a 60 Hz power system consists primarily of a tone at 120 Hz.

The A-weighted measurement or sound-pressure level shall be used to determine the average sound level performance of a dry-type air-core series reactor. The procedures specified for measuring reactor sound-pressure levels are intended to be applicable to reactors being tested indoors or outdoors at the factory or to those that have been installed in the field.

9.10.1 Instrumentation

Sound-Pressure level measurements shall be made with instrumentation that meets the requirements of ANSI S1.4-1983 for type 2 meters. A suitable wind screen shall be used when the air velocity due to winds causes the readings to be in error. Sound-Measuring instrumentation shall be calibrated before and after each measurement session. Further, it should be demonstrated prior to the measurement that the magnetic field of the reactor does not affect the rating of the sound level meter. Should the calibration change by more than 1 dB due to the magnetic field, the measurements shall be declared invalid.

9.10.2 Test conditions

Measurements should be made in an environment having an ambient sound-pressure level at least 5 dB below the combined sound-pressure level. When the ambient sound-pressure level is 5 dB or more below the combined level of reactor and ambient, the corrections shown in Table 6 shall be applied to the combined reactor and ambient sound pressure level to obtain the reactor sound-pressure level. When the difference between the reactor sound-pressure level and the ambient sound-pressure level is less than 5 dB, and it is only desired to know the sound-pressure level that the reactor does not exceed, a correction of -1.6 dB may be used.

Difference between average sound level of combined series reactor and ambient and average sound level of ambient (dB)	Correction to be applied to average sound level of combined series reactor and ambient to obtain average sound level of series reactor (dB)
5	1.6
6	1.3
7	1.0
8	0.8
9	0.6
10	0.4
Over 10	0.0

Table 6. Correction to sound level

When ambient sound conditions do not comply with the above, suitable corrections may be feasible when the ambient sound conditions are steady. For this condition, the details and method for making the measurements and the ambient corrections shall be agreed upon by those responsible for the design and application of the reactor.

The reactor shall be located so that no acoustically reflecting surface is within 3 m (10 ft) of the measuring microphone, other than the floor or ground. Should the reactor be tested within a semireverberant facility, it should be located in an asymmetrical manner with respect to the room geometry. If the specified conditions cannot be met, the measurement results may not be valid. When reactor sound emissions are measured in an enclosed space, sound reflections from walls or other large objects can influence the results because the sound is essentially a discrete tone that may be affected by room acoustics, room geometry, or reflecting objects. Thus, there may be differences in the sound measured in an indoor reactor or outdoor reactor installation.

The reactor shall be energized at rated current with rated frequency. If the reactor is designed with means for adjusting the impedance, it should be set for rated impedance.

Three-Phase series reactors shall be energized from a three-phase source and single-phase series reactors from a single-phase source. When available test power is insufficient for testing at rated current, then the manufacturer must demonstrate to the user’s satisfaction that reduced-current testing produces sufficiently accurate results when extrapolated to the rated current level. If this cannot be demonstrated to the user, a field test can be performed.

Sound measurements shall begin after the reactor being tested is energized and steady-state sound level conditions are established. Measurements may be made immediately on reactors that have been in continuous operation.

When sound-level tests are made at the factory, the mounting conditions that are to be utilized at the final installation should be simulated as much as practicable.

9.10.3 Microphone positions

The reference sound-producing surface of a dry-type air-core reactor is its outside winding surface.

For single-phase reactors with a winding less than 2.4 m (8 ft) tall, microphone locations shall be at mid-height of the winding. For single-phase reactors greater than 2.4 m tall, microphone locations shall be at one-third and two-thirds of the winding height. For two- and three-coil stacked arrangements, microphone locations shall be at mid-height of each reactor winding. If measurements at the above heights are not possible due to bus bar layout, microphone locations shall be at the mid-height of the base reactor winding. In plan view, the microphone locations shall be laid out clockwise, sequentially along the circumference of a circle having its center at the geometric center of the reactor, and a radius equal to the reactor radius plus 3 m (10 ft). The first station will be on a radial line through the bottom terminal, or as close to it in the clockwise direction as is permitted to comply with minimum clearance distances to live parts.

For side-by-side arrangements of single or stacked reactors, microphone locations are determined by the same method as for a single coil or single stack, if the locations do not overlap. If the microphone locations do overlap, measurements shall only be taken around the outermost perimeter of the resulting contour (see Figure 4).

9.10.4 Sound-Level measurement

Sound-Pressure levels shall be measured in conformance with IEE Std C57.16-1996 using the sound-level meter A-weighting characteristic.

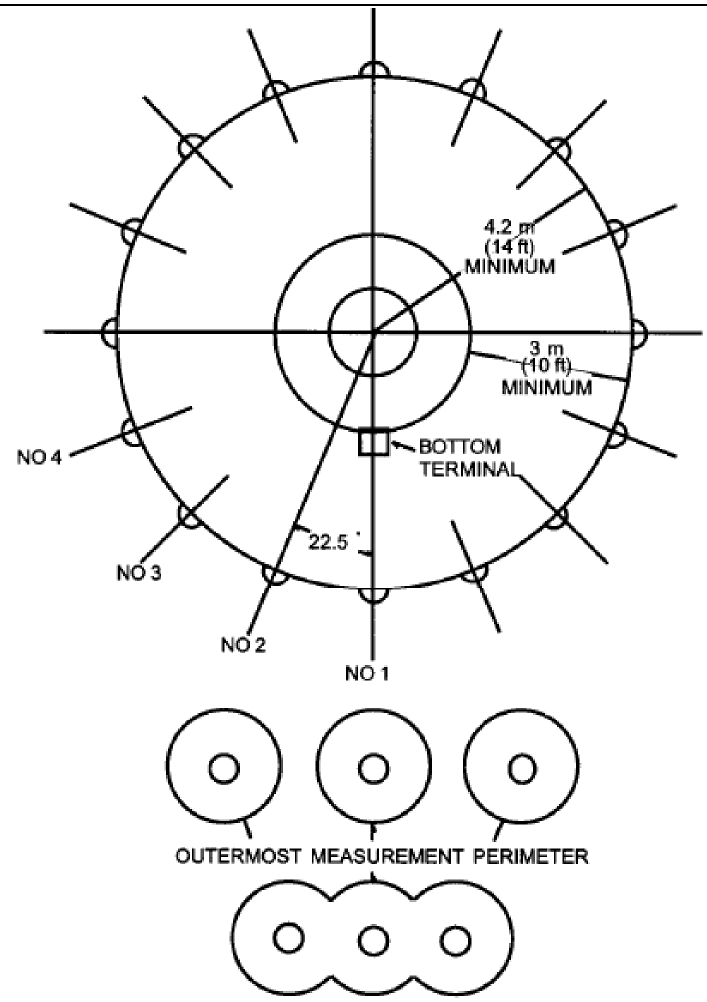


Fig. 4 – Microphones locations for audible sound tests

9.10.5 Calculation of average sound level

An average sound level value L_A shall be calculated from the measured values of the A-weighted sound level L_A by using the following equation:

$$L_A = 10\log_{10}\left(\frac{1}{N}\sum_i 10^{0.1L_{Ai}}\right) \text{-------------------} \quad (10)$$

where
L_A is the average sound level in decibels,
L_{Ai} is the measured sound level at location *i* in decibels, and
N is the total number of measurement locations.
It should be noted that the above calculated value may have to be corrected for the following factors:

- Ambient noise level
- Acoustic characteristics of the location where sound readings are taken, e.g., reverberant properties of the test lab

10. Performance Criteria

Routine tests including measurement of inductance and losses and the performance of a turn-to-turn or impulse dielectric test, at 100% specified voltage, should be carried out on the Fault Current Limiting reactors before and after the short-circuit test. Inductance and loss values should be consistent with measurement tolerance limits. Oscillograms from the required dielectric test should show no change, agreeing with the limits of the high-voltage dielectric test systems.

11. Additional IEEE C57.12.01-2005 Recommended Tests.

Tests in this standard are meant for dry type transformers but are included here as part of the ZENERGY Power FCL testing procedure since they have been identified as part of the SCE Field Testing Acceptance Criteria.

Tables 7 through 9 show the relevant tests in accordance with IEEE Std C57.12.01-2005.

11.1 Dielectric Insulation

Nominal L-L system voltages	Low-frequency voltage insulation level[a]	Basic lighhtning impulse insulation levels (BIL ratings) in common use kV crest[b,c] (1.2 x 50 microsec)									
(kV)	(kV rms)	10	20	30	45	60	95	110	125	150	200
0.25	2.5	None									
0.6	3	S[d]	I[e]	I							
1.2	4	S	I	I							
2.5	10		S	I	I						
5.0	12			S	I	I					
8.7	19				S	I	I				
15.0	**34**					S	I	I			
18.0	40						S	I	I		
25.0	50						2[f]	S	I	I	
34.5	70								2	S	I
Chopped wave[g,h] minimum time to flashover µs		1.0	1.0	1.0	1.25	1.5	1.6	1.8	2.0	2.25	2.7

CAUTION
When impulsing the low side windings, the high side may experience relatively higher voltages than BIL levels.

NOTE—The latest edition of IEEE Std C62.22 should be consulted for information coordination with available surge arrester protection levels.

[a] Low-frequency voltage insulation levels apply to the standard "S" levels in the table.
[b] Low-impedance low-side windings may be tested with a much faster 0.5 × 1.5 µs impulse wave on BIL ratings less than or equal to 30 kV.
[c] A positive impulse wave shall be used.
[d] S = Standard values.
[e] I = Optional higher level where exposure to overvoltages occurs and improved protective margins are required.
[f] 2 = Optional lower levels where protective characteristics of applied surge arresters have been evaluated and found to provide appropriate surge protection.
[g] The voltage crest of the chopped wave should be approximately the same as the full wave magnitude.
[h] No chopped waves are required on 0.6 kV systems and below.

Table 7. Dielectric insulation levels for dry-type transformers used on systems with BIL ratings 200 kV and below

11.2 Partial Discharge

Standard voltage class (kV)	Pre-stress voltage level (kV L-L)	Maximum permissible partial discharge intensity @110% rated voltage in pC
0.25	—	—
0.6	0.8	50
1.2	1.6	50
2.5	3.3	50
5.0	6.5	50
8.7	11.3	100
15.0	**19.5**	**100**
18.0	23.4	100
25.0	32.5	100
34.5	44.9	100

Table 8. Partial discharge limits and pres-stress limits

11.3 Miscellaneous dry-type transformer tests

Tests	Test classification					
	≤500 kVA			≥501 kVA		
	Routine	Design	Other	Routine	Design	Other
Resistance measurements of all windings on the rated voltage tap, and at tap extremes of the first unit made on a new design	—	x	—	x	—	—
Ratio tests on the rated voltage connection	x	—	—	x	—	—
Polarity and phase relation tests on the rated voltage connection	x	—	—	x	—	—
No-load losses and excitation current at rated voltage on the rated voltage connection	x[a]	—	—	x	—	—
Impedance voltage and load loss at rated current and rated frequency on the rated voltage connection and at the tap extremes of the first unit of a new design	—	x	x	x	—	—
Temperature rise at minimum and maximum ratings of the first unit on a new design. This test may be omitted if tests of thermally duplicate or essentially duplicate unit are available	—	x	x	—	x	x
Dielectric tests						
Applied voltage	x	—	—	x	—	—
Induced voltage	x	—	—	x	—	—
Impulse	—	x[b]	x[b]	—	x[b]	x[b]
Insulation power factor	—	—	**x**	—	—	x
Insulation resistance	—	—	**x**	—	—	x
Partial discharge	**x[c]**	—	x[c]	x[c]	—	x[c]
Audible sound level	—	x	x	—	x	x
Short-circuit capability	—	—	x	—	—	x
Mechanical (for sealed transformers)						
Pressure	—	x	—	—	x	—
Leak	x	—	—	x	—	—

[a]Statistical sampling may be used for this test. (This does not apply to transformers ≥501 kVA.)
[b]When an impulse test is required, it shall precede the applied and induced voltage test.
[c]Partial discharge tests may be performed on the windings of all types of dry-type transformers, but they are considered routine tests for transformers above 1.2 kV having solid-cast and/or resin-encapsulated windings as part of the insulation systems

Table 9. Dry type transformer tests

12. Conclusions

The test protocol for the ZENERGY Power Fault Current Limiter is presented. Tests are fundamentally based on IEEE relevant standards that address test codes for dry-type air-core series-connected reactors and dry-type distribution and power transformers, including those with solid cast and/or resin encapsulated windings

Some of the described tests are regarded as optional and should be conducted only when required by buyers.

13. List of Tables and Figures

List of Revisions

Revision	Date	Action	Modified Page
1	05/05/08	Released	
2	07/14/08	Added Table 1. Changed ms to μs in last paragraph of section 9.7	page 4 page18

APPENDIX B:
Zenergy Power HTS FCL Laboratory Test Report

Test Report

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Responsible Person:	Franco Moriconi				
Project Name:	High Temperature Superconducting Fault Current Limiter				
Document Title:	**High Voltage Testing – Powertech Labs, Surry BC Canada**				
Document Ref.No.:	SCP/TR-07/03	Reg: #		Page 1	
Date of issue:	12/31/07	Classification:	Confidential	No. of pages:	21
Client(s):	SC Power				
Author(s):	F. Moriconi	Approved:	Bert Nelson	Order No.:	
Distribution:	Frank Lambert (NEETRAC), Lloyd Cibulka (CEC), Keyue Smedley (CEC), Alan Hood (SCE), Victor Gore (SCE), Chris Rose (LANL), Bert Nelson (SCP), Woody Gibson (SCP), Carsten Bührer (Zenergy), Frank Darmann (AS), William Boettger (SCP), William Schram (SCP), Larry Masur (SCP), Randy Proctor (SCP), Alonso Rodriguez (SCP), Stewart Ramsay (SCP), Amadeep Singh (SCP)				
Distribution page 1:					
Keywords:	Fault current limiter, high temperature superconducting				

Summary:

The report presents the results obtained during high voltage testing of our inductive type High-Temperature Superconducting (HTS) Fault Current Limiter (FCL) performed from December 10, 2007 through December 14, 2007 at Powertech Labs in Surry, British Colombia Canada.
SCP first large-scale HTS FCL is a three-phase device that is designed to operate at 12.47 kV and 1,200 amps steady-stated current, and to be able to clip a 10,000 to 12,000 kA prospective fault current by 10% to 15% for multiple, rapidly reoccurring faults of up to 30 cycles (1/2 second) in duration.
The scope of this work was to measure the FCL capability of clipping a 10-12 kA RMS prospective fault current when operating under nominal conditions at 13kV and 1200A steady state current.

The results show a 22% fault current clipping capability for a 16kA prospective fault, and 20% clipping capability for a 10kA prospective fault current. The peak short circuit current was reduced by 23% for the highest fault current settings of 16kA.

A summary table of all tests performed is given in section 6 of the report. The test set up is illustrated in section 6. A fault current characterization test, with the FCL out of circuit, was initially performed in order to determine the appropriate source impedance values capable of generating prospective fault current RMS levels of 12,500, 10,000, 5,000 and 2,500 amperes, with an X/R ratio of approximately 10-11.
Section 8 presents the results of the short circuit test with the FCL in circuit. Section 9 summarizes the fault clipping capability of our FCL. RMS and peak fault current values are tabulated and plotted for every fault current setting and phase.

Contents **Page**

1. General

The report presents the results obtained during high voltage testing of our inductive type high-temperature superconducting (HTS) fault current limiter (FCL) performed from December 10, 2007 through December 14, 2007 at Powertech high-power test facility in Surry, British Colombia Canada. SCP first large-scale HTS FCL is a three-phase device that is nominally designed to operate at 12.47 kV and 1,200 amps steady-stated current, and to be able to clip a 10,000 to 12,000 kA prospective fault current by 10% to 15% for multiple, rapidly reoccurring faults of up to 30 cycles (1/2 second) in duration.

The test set up is illustrated in section 6 of this report. A fault current characterization test, with the FCL out of circuit, was initially performed in order to determine the appropriate source impedance values capable of generating prospective fault current RMS levels of 12,500, 10,000, 5,000 and 2,500 amperes, with an X/R ratio of approximately 10-11. Reactive and resistive source impedance components available at Powertech are given in figures 2 and 3. The appropriate resistive loads RL were connected in Delta configuration to generate a steady state current of approximately 1200 amps. The list of available resistive components is given in figure 4. The results of the fault current characterization test with the FCL out of circuit are presented in section 7 of this report.

The FCL was then connected in series with the circuit as shown in figure 1 and a three phase short circuit was generated with an auxiliary vacuum circuit breaker. A zero voltage crossing point on wave was implemented on phase A. The main circuit breaker and auxiliary breaker pulse intervals were adjusted to generate 10-12 cycles of steady state current prior to fault, 12 cycles of short circuit conditions, and 10-12 cycles of steady state return prior to shut down. The total event was approximately 600 msec.
The test was repeated for every combination of source impedance as defined by the fault current characterization test. A list of all short circuit and calibration tests is given in figure 5.

Section 8 of this report presents the results of the short circuit test with the FCL in circuit, for prospective fault current RMS levels of 2.5, 5, 10, and 12.5 kA. The 12.5 kA impedance settings was underestimated and the actual fault current level was measured at 16kA. Figure 10 shows a table with the test settings, the values of RMS steady state current and RMS fault currents for every phase, the fault peak values, and the measured X/R ratios.

Section 9 summarizes the fault clipping capability of our FCL. RMS and peak fault current values are tabulated and plotted for every fault current setting and phase.
Figure 18 shows a 22% fault current clipping capability for a 16kA prospective fault and 20% clipping capability for a 10kA prospective fault current. The peak short circuit current was reduced by 23% for the highest fault current settings of 16kA.

2. Scope

The scope of this work was to measure the FCL capability of clipping a 10-12 kA RMS prospective fault current when operating under nominal conditions at 13kV and 1200A steady state current.

3. Applicability

High temperature superconducting fault current limiter.

4. Applicable documentation

SCP/TR-07/001, Test Report “FCL Test Results PG&E San Ramon”
FCL Functional testing schedule Rev 01 Nov 27 2007 (in appendix)

5. Acronyms and definitions

5.1 Acronyms

FCL	Fault Current Limiter
HTS	High Temperature Superconductor
SC	Super Conductor
DC	Direct Current
AC	Alternating Current
EMF	Electro Magnetic Force
HV	High Voltage
PT	Power Transformer
CT	Current Transformer
VD	Voltage Divider

5.2 Definitions

Xs	Reactive part of source impedance
Rs	Resistive part of source impedance
RL	Resistive load
TFR	Transformer
AUX	Auxiliary (circuit breaker for bolted 3-phase short circuit)
X/R	Reactive over resistive impedance ratio
Ia, Ib, Ic	Nominal current RMS, phase a, b and c
I_ss	Steady state current RMS
I_sc	Short circuit current - RMS
I_peak	Short circuit current - Peak

6. Powertech Lab setup - High Voltage Testing

The test set up is illustrated below in Figure1. Reactive and resistive source impedance components available at Powertech are given in figures 2 and 3. The appropriate resistive loads RL were connected in Delta configuration to generate a steady state current of approximately 1200 amps. The list of available resistive components is given in figure 4. A list of all short circuit and calibration tests is given in figure 5.

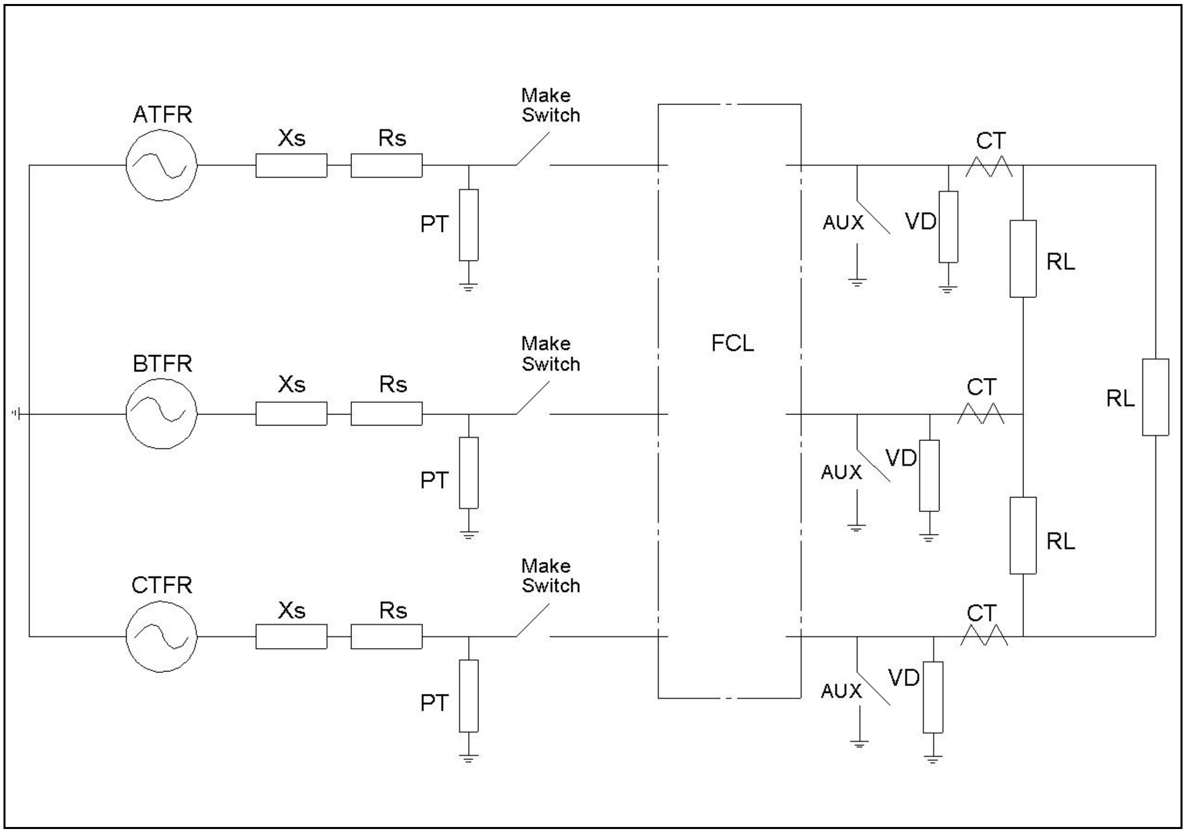

Fig. 1: PowerTech Test Schematic

No.	Reactance @60 Hz at phase			Maximum Current		One shot I2t @30C	X/R at 20C	Continuous current
#	A	B	C	kArms	kApeak	A2s	-	Arms
1	0.0021	0.0022	0.0021	84.7	244	3.8E+11	95	4000
2	0.0044	0.0042	0.0040	84.9	237	1.8E+11	90	4000
3	0.0083	0.0082	0.0082	80.2	224	1.2E+11	89	4000
4	0.0165	0.0166	0.0165	72.2	201	5.0E+10	84	3000
5	0.0320	0.0339	0.0325	60.2	168	2.2E+10	69	2700
6	0.0630	0.0671	0.0609	45.2	126	1.1E+10	79	1900
7	0.1316	0.1292	0.1315	32.0	89	5.8E+09	75	1900
8	0.2590	0.2640	0.2590	23.0	64	4.2E+09	89	1100
9	0.5300	0.5180	0.5210	16.4	46	1.8E+09	94	750
10	1.0400	1.0290	1.0360	11.6	32	7.6E+08	79	450
11	2.1000	2.0700	2.1000	7.5	21	4.8E+08	82	300
12	4.2200	4.2100	4.2300	4.5	12	2.0E+08	82	220
13	8.3900	8.3100	8.3100	2.5	7	1.2E+08	83	160
14	16.9200	17.0900	16.9600	1.3	4	5.8E+07	83	110
15	33.6900	34.3500	34.1000	0.7	2	3.0E+07	77	80
Sum 1-13	16.80	16.66	16.71	-	-	-	-	

Fig. 2: Source Reactance Values

	mOhms	kA	MJ
R1	4.5	20	16
R2	8.5	20	32
R3	18.1	20	64
R4	31.3	20	72
R5	70.2	20	144
R6	122	20	128
R7	269	18.3	144
R8	488	9.3	128
R19	888	4.6	144
R10	2132	2.3	128
R11	4247	1.2	64

Fig. 3: Source Resistor Values

Name	A phase Ohms	B phase Ohms	C phase Ohms	Energy J	Imax Arms	Icont Arms
LR1	2.06	2.08	2.08	6.0E+06	750	105
LR2	4.16	4.16	4.19	1.2E+07	750	105
LR3	8.27	8.35	8.38	2.4E+07	750	105
LR4	16.80	16.92	16.77	4.8E+07	750	105
LR5	29.50	29.70	29.60	6.0E+07	600	85
LR6	63.00	63.10	63.20	3.0E+07	300	50

Fig. 4: Load Resistor Values

Test/Shot	Date/Time	Mimic	Test Record	Ia	Ib	Ic	Pulse 1	Pulse 2	Pulse 3	Notes	FCL
#		kV	#	kA rms	kA rms	kA rms	msec	msec	msec		
Cal_1	Dec 12/7:50	13.1	1	2.5	2.49	2.45				X/R = 11.2	Out
Cal_2	Dec 12/8:02	13.1	2	4.89	5.01	4.9				X/R = 11.1	Out
Cal_3	Dec 12/8:14	13.1	3	9.84	9.91	9.72				X/R = 10.7	Out
Cal_4	Dec 12/10:00	13.1	4	2	2	2					Out
Cal_5	Dec 12/10:07	13.1	5	1.28	1.26	1.26				10kA / 1200A	Out
Cal_6	Dec 12/10:19	13.1	6	1.37	1.36	1.36				5kA / 1200A	Out
Cal_7	Dec 12/10:29	13.1	7	1.48						3,1	Out
Cal_8	Dec 12/10:34	13.1	8	1.32	1.32	1.31					Out
Cal_9	Dec 12/10:53	13.1	9	2.5	2.49	2.45					Out
Cal_10	Dec 12/10:59	13.1	10	4.89	5.01	4.9					Out
Cal_11	Dec 12/11:03	13.1	11	9.84	9.91	9.72					Out
Cal_12	Dec 12/11:59	13.1	12	-	-	-	200	250	150	timing	Out
Cal_13	Dec 12/12:06	13.1	13	1.14	1.12	1.11	191	253	164	10kA / 1200A	Out
Cal_14	Dec 12/12:18	13.1	14	1.1	1.08	1.07	192	252	165	5kA / 1200A	Out
Cal_15	Dec 12/12:25	13.1	15	1.08	1.07	1.07	193	251	165	2.5kA / 1200A	Out
1/1	Dec 12/14:51	13.1	16	0.98	0.97	0.97	193	251	165	Sparks Started Video recording	In
Cal_16	Dec 12/15:53	13.1	17	0.98	0.97	0.97				1 sec steady state	In
Cal_17	Dec 12/16:14	13.1	18	0.98	0.97	0.97				Removed Top L brakets only Fewer fault cycles Sparks	In
Cal_18	Dec 12/17:17	13.1	19	0.98	0.97	0.97				Removed all top brakets Sparks	In
Cal_19	Dec 13/9:43	13.1	20	0.98	0.97	0.97	100			OK No Sparks 6 cycles 1100A steady state	In
Cal_20	Dec 13/9:52	13.1	21	0.98	0.97	0.97	500			OK No Sparks 30 cycles 1100A steady state	In
1/2	Dec 13/10:07	13.1	22	0.98	0.97	0.97	193	251	165	2.5kA / 1200A No Sparks	In
2/1	Dec 13/10:30	13.1	23	1.03	1.01	0.99	193	251	165	4.2kA / 1200A Sparks	In
2/2	Dec 13/10:45	13.1	24	1.03	1.01	0.99	193	251	165	4.2kA / 1000A Turned off flash light Sparks	In
3/1	Dec 13/11:10	13.1	25	1.08	1.06	1.04	193	251	165	10kA / 1000A 7.86,7.83,7.7	In
Cal_21	Dec 13/11:50	13.1	26	7.89	6.95	7.46	100				In
4/1	Dec 13/13:45	13.1	27	7.89	6.95	7.46	500				In
4/2	Dec 13/14:00	13.1	28				193	50	-	7A / 10kA	In
4/3	Dec 13/14:04	13.1	29	7900	7860	7720	193	253	165	7A / 10kA Sparks	In
4/4	Dec 13/14:18	13.1	30	7900	7860	7720	193	253	165	7A / 10kA Sparks	In
4/5	Dec 13/14:26	13.1	31	7900	7860	7720	193	253	165	7A / 10kA Sparks	In
Cal_22	Dec 13/14:43	13.1	32	1100	1090	1070	100				In
5/1	Dec 13/14:50	13.1	33	12700	12800	12500	193	253	165	12.5kA / 1100A HTS COIL ON	In
5/2	Dec 13/15:01	13.1	34	12700	12800	12500	193	253	165	12.5kA / 1100A HTS COIL OFF	In
Cal_23	Dec 14/8:29	13.1	35	1140	1120	1120				Load only	Out
Cal_24	Dec 14/9:22	13.1	36	16200	16500	16100				Source only X/R = 6.8	Out

Fig. 5: Table - Test summary

7. Fault Current Characterization – FCL out of circuit

A fault current characterization test was performed in order to determine the appropriate source impedance values capable of generating prospective fault current RMS levels of 12,500, 10,000, 5,000 and 2,500 amperes, with an X/R ratio of approximately 10-11. The test with 12.5kA settings was performed in two steps, the first one to characterize the load and the second one to characterize the fault current.

The 12.5 kA impedance settings was underestimated and the actual fault current level was measured at 16kA.

Test Record	KV	Isc kA	Iss kA	Ia_ss kA	Ib_ss kA	Ic_ss kA	Ia_sc kA	Ib_sc kA	Ic_sc kA	X/R	Ia_peak kA	Ib_peak kA	Ic_peak kA	Notes	FCL
15	13.1	2.5	1.2	1.08	1.07	1.07	2.5	2.49	2.45	11.2	4.84	5.25	3.85		Out
14	13.1	5	1.2	1.1	1.08	1.07	4.9	5.0	4.9	11.1	10.80	10.40	8.00		Out
13	13.1	10	1.2	1.14	1.12	1.11	9.6	9.6	9.6	10.7	23.20	19.00	17.40		Out
35	13.1	-	1.2	1.14	1.12	1.12	-	-	-	-	-	-	-	Load only	Out
36	13.1	12.5	-	-	-	-	16.2	16.5	16.1	6.8	39.30	26.60	31.40	Source only	Out

Fig. 5: Fault Current Characterization tests

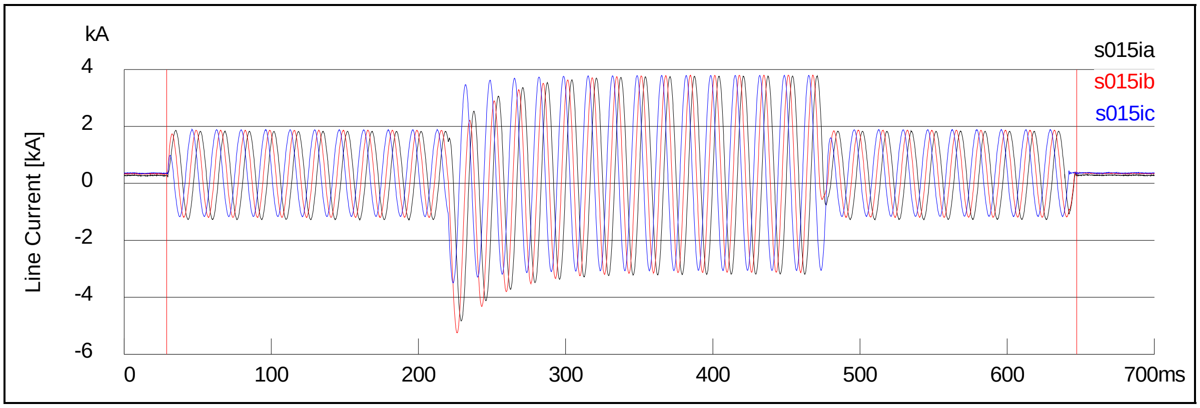

Fig. 6: 2.5 kA Fault Current Characterization

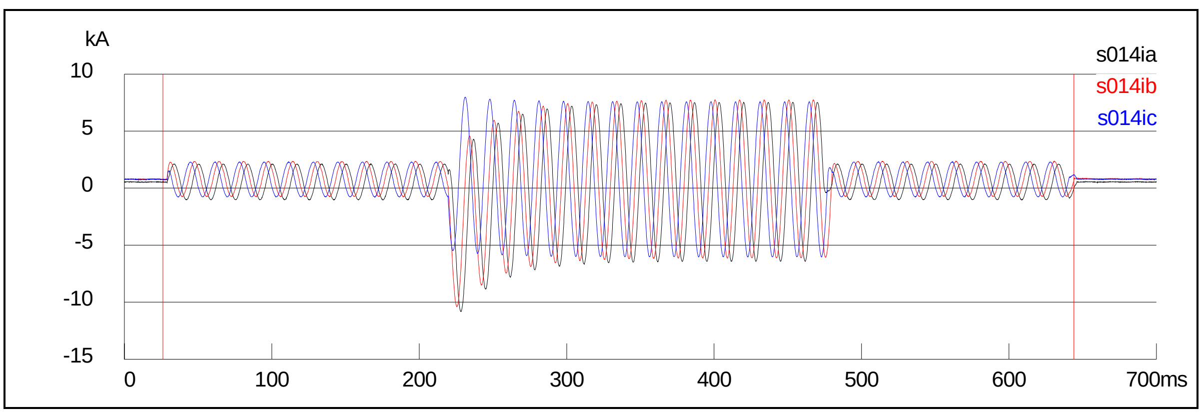

Fig. 7: 5 kA Fault Current Characterization

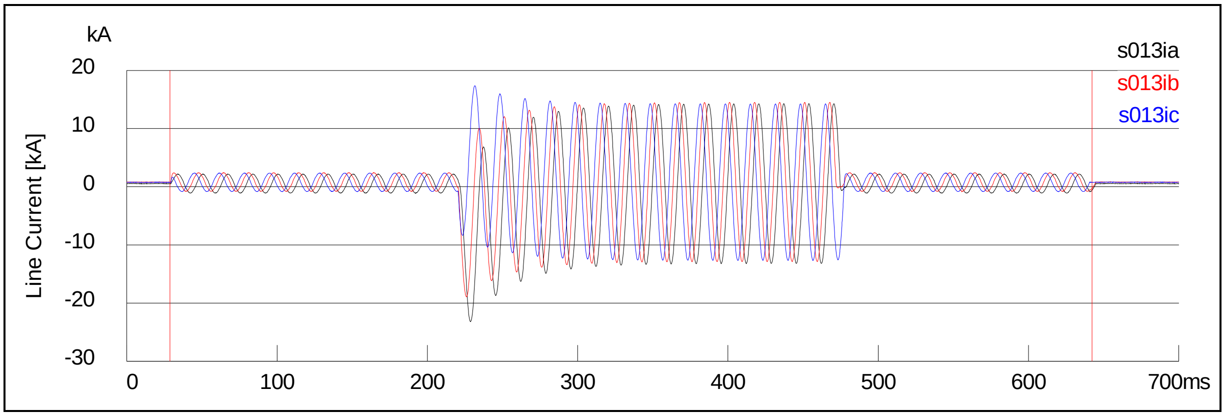

Fig. 8: 10 kA Fault Current Characterization

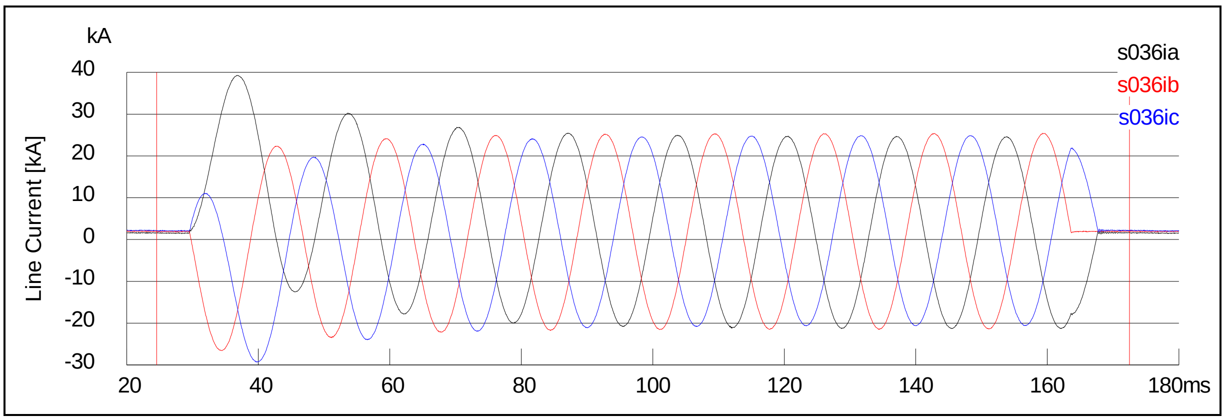

Fig. 9: 12.5 kA Fault Current Characterization

8. Fault Current tests – FCL in circuit

The FCL was connected in series with the line and a three phase short circuit was generated with an auxiliary vacuum circuit breaker. A zero voltage crossing point on wave was implemented on phase A. The main circuit breaker and auxiliary breaker pulse intervals were adjusted to generate 10-12 cycles of steady state current prior to fault, 12 cycles of short circuit conditions, and 10-12 cycles of steady state return prior to shut down. The total event was approximately 600 msec. The test was repeated for every combination of source impedance as defined by the fault current characterization test.

Test Record	KV	Isc kA	Iss kA	Ia_ss kA	Ib_ss kA	Ic_ss kA	Ia_sc kA	Ib_sc kA	Ic_sc kA	X/R	Ia_peak kA	Ib_peak kA	Ic_peak kA	FCL
22	13.1	2.5	1.2	0.98	0.97	0.97	2.1	2	2	11	4.2	4.95	3.62	In
23	13.1	4.2	1.2	1.15	1.28	1.24	4.16	4.17	4.05	11	9.5	10.9	6.6	In
24	13.1	4.2	1.0	1.03	1.01	0.99	4.22	4.19	4	11	9.7	10.8	5.9	In
25	13.1	10	1.0	1.08	1.06	1.04	7.85	7.85	7.7	10.6	18	20.4	13.5	In
33	13.1	12.5	1.1	1.1	1.08	1.08	12.7	12.8	12.5	6	25.5	30.3	23.9	In

Fig. 10: Fault Current Tests – summary table

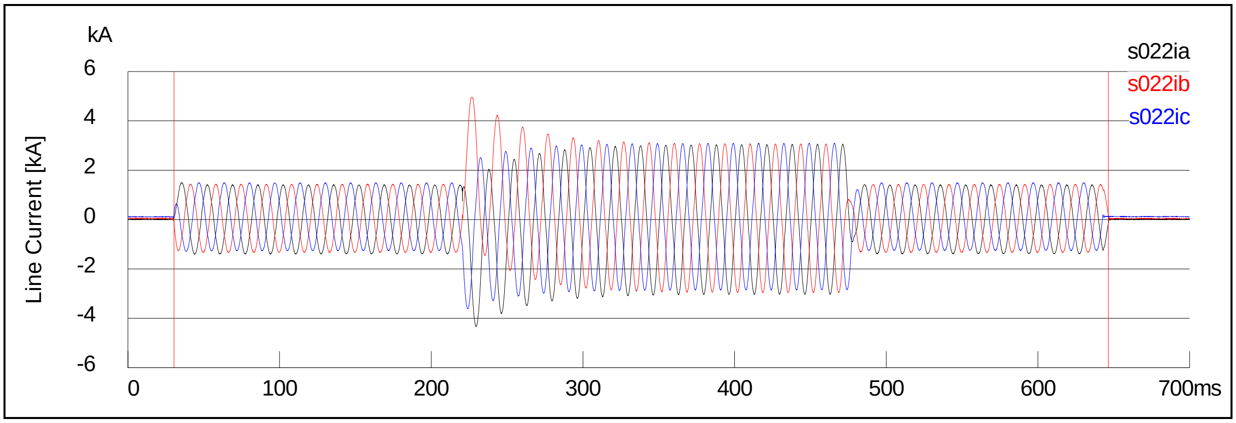

Fig. 11: 2.5kA Fault Current Test

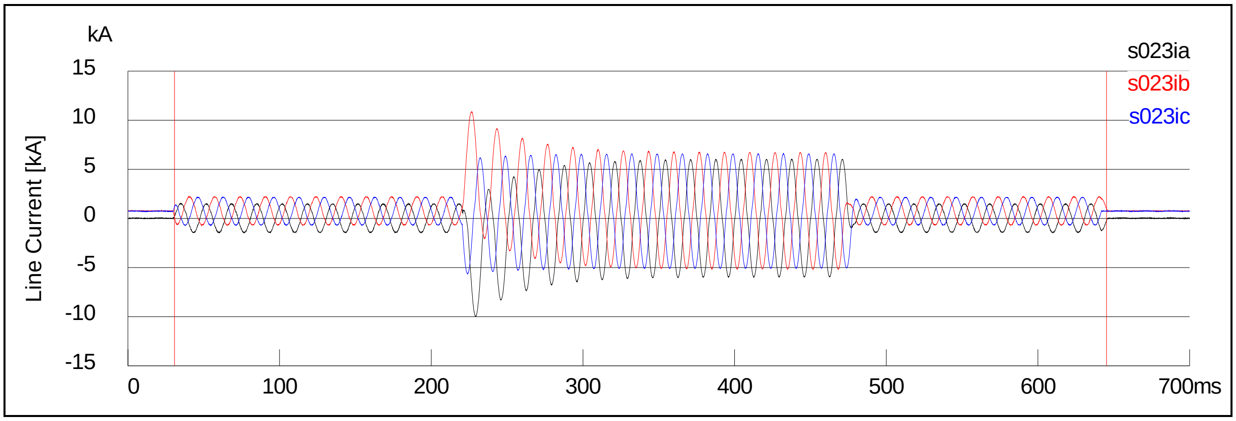

Fig. 12: 5kA Fault Current Test

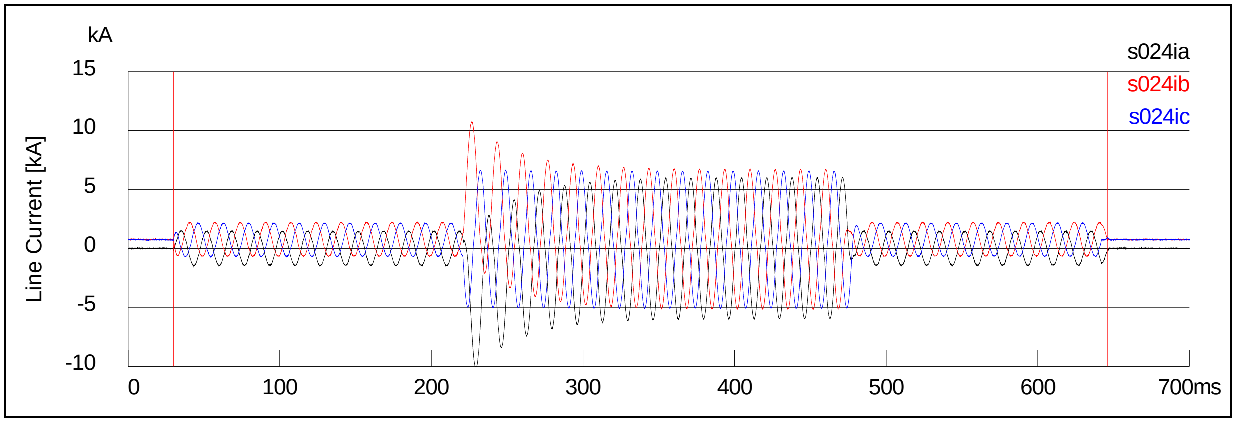

Fig. 13: 5kA Fault Current Test - Repeat

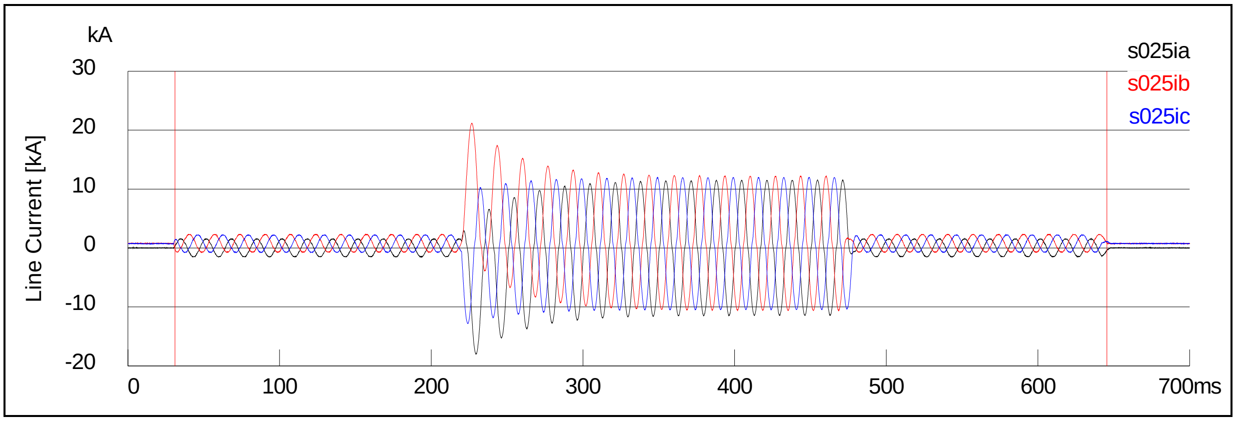

Fig. 14: 10kA Fault Current Test

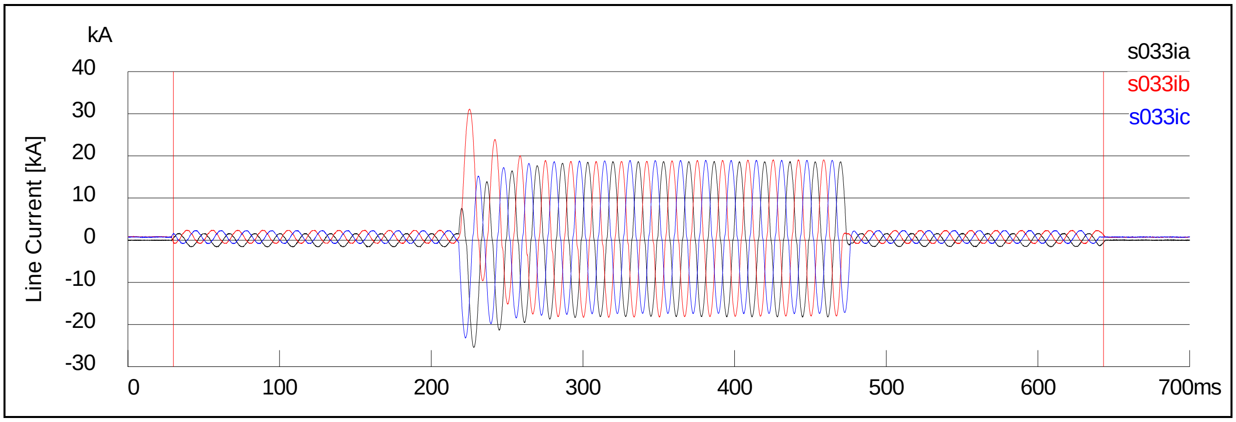

Fig. 15: 12.5kA Fault Current Test

9. FCL clipping capability

The FCL clipping capability is reported below. RMS and peak fault current values are tabulated and plotted for every fault current setting and phase.
Figure 18 shows a 22% fault current clipping capability for a 16kA prospective fault and 20% clipping capability for a 10kA prospective fault current. The peak short circuit current was reduced by 23% for the highest fault current settings of 16kA.

		FCL OUT			FCL IN			Fault Current Clipping	FCL OUT			FCL IN			Peak Current Reduction
KV	Isc kA	Ia_sc	Ib_sc	Ic_sc	Ia_sc	Ib_sc	Ic_sc	%	Ia_peak	Ib_peak	Ic_peak	Ia_peak	Ib_peak	Ic_peak	%
13.1	2.5	2.5	2.49	2.45	2.1	2	2	14%	4.84	5.25	3.85	4.2	4.95	3.62	6%
13.1	5	4.9	5.0	4.9	4.22	4.19	4	14%	10.80	10.40	8.00	9.7	10.8	5.9	0%
13.1	10	9.6	9.6	9.6	7.85	7.85	7.7	20%	23.20	19.00	17.40	18	20.4	13.5	12%
13.1	16	16.2	16.5	16.1	12.7	12.8	12.5	22%	39.30	26.60	31.40	25.5	30.3	23.9	23%

Fig. 17: FCL Clipping capability – Results table

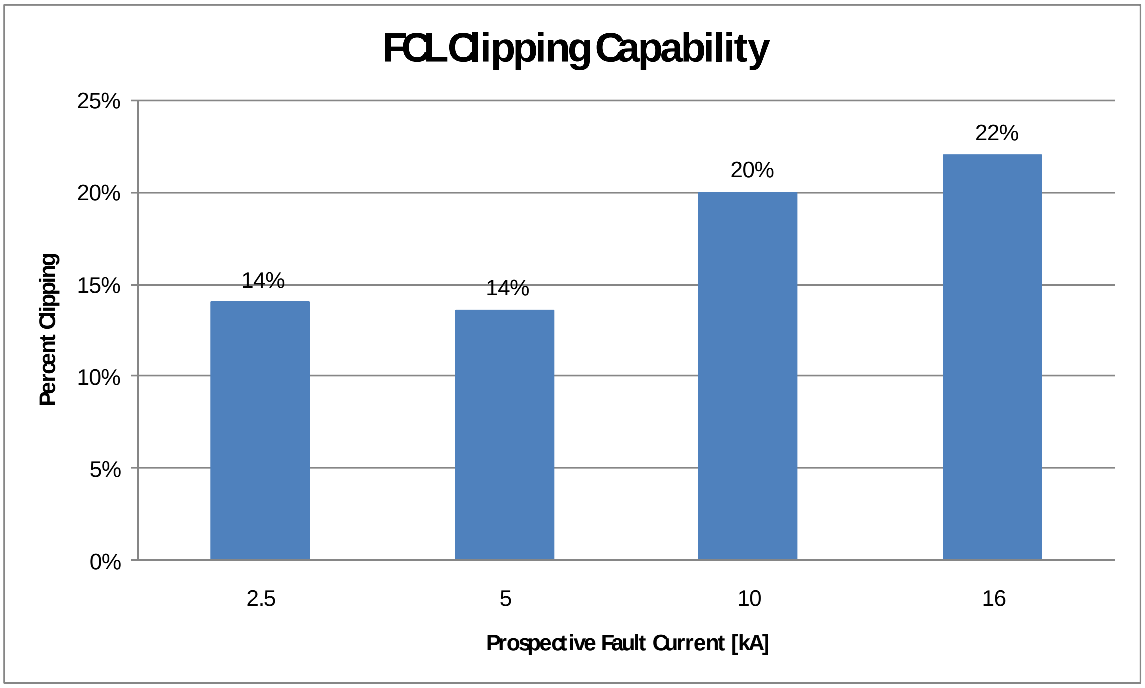

Fig. 18: FCL Clipping capability – percent vs. fault current levels

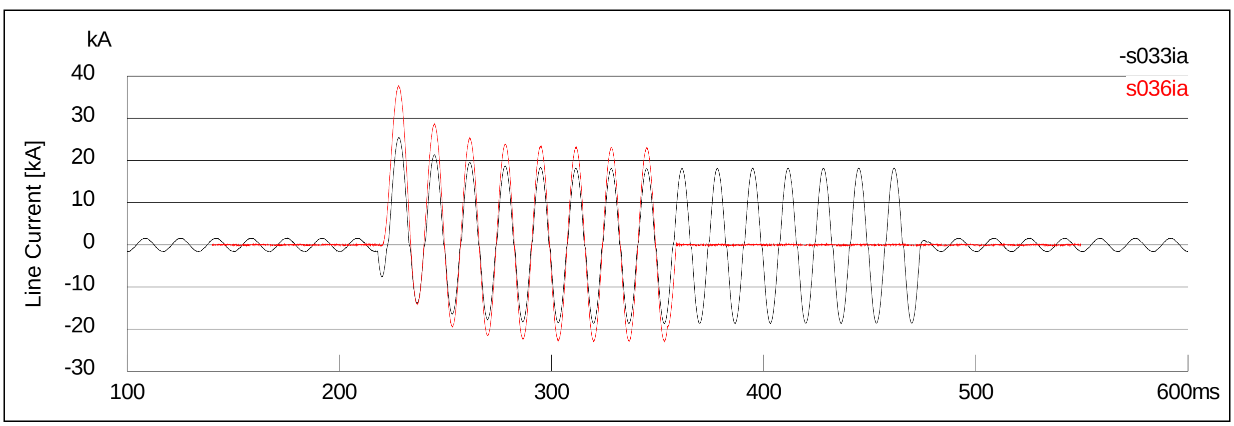

Fig. 19: 16kA Fault current – FCL In vs. Out – phase A

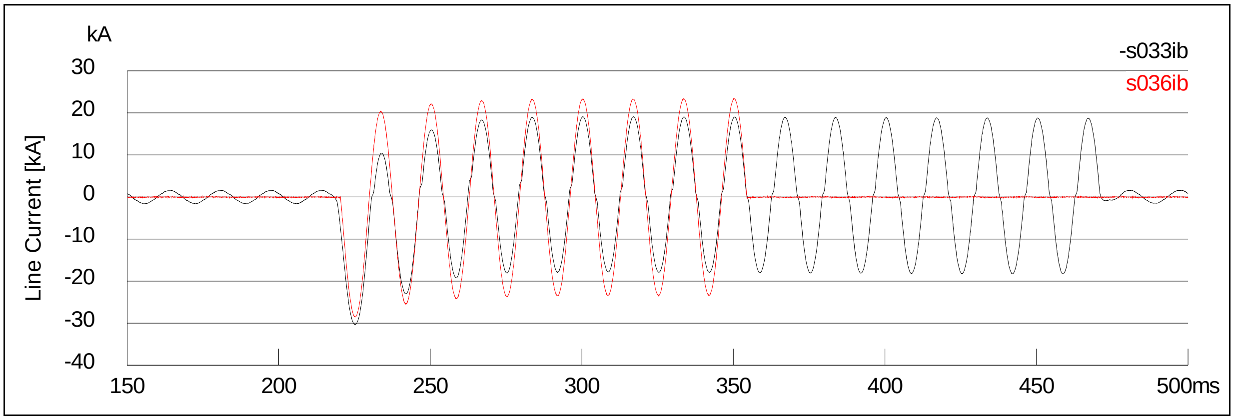

Fig. 20: 16kA Fault current – FCL In vs. Out – phase B

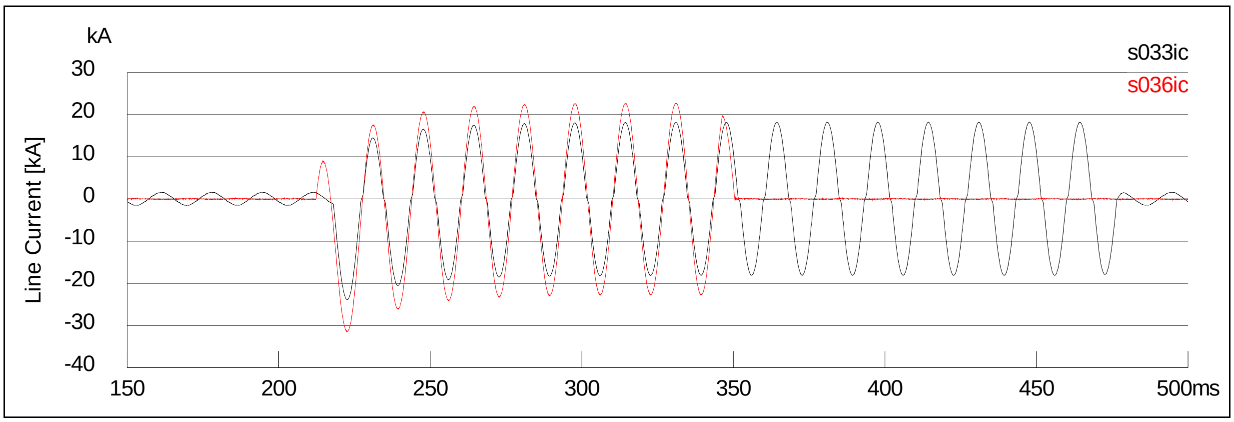

Fig. 21: 16kA Fault current – FCL In vs. Out – phase C

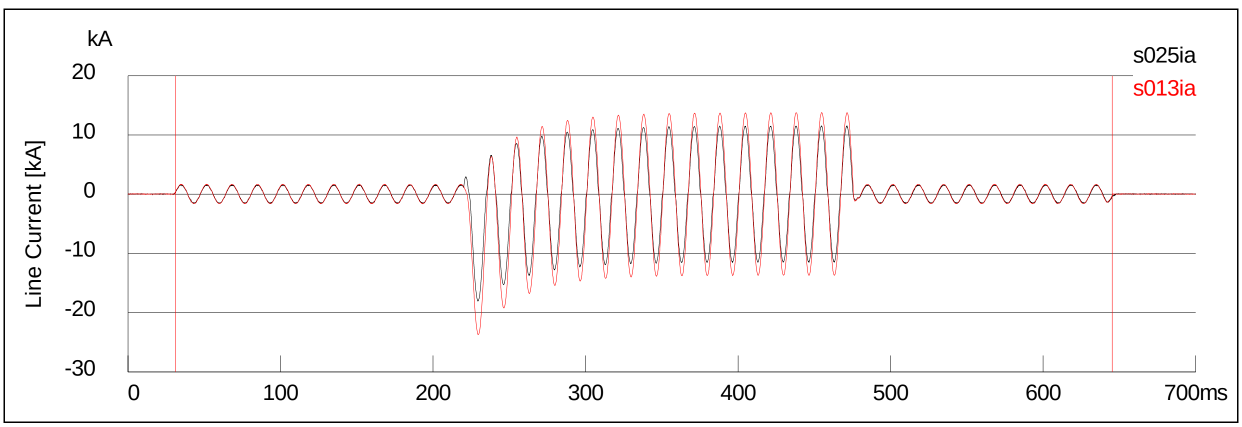

Fig. 22: 10kA Fault current – FCL In vs. Out – phase A

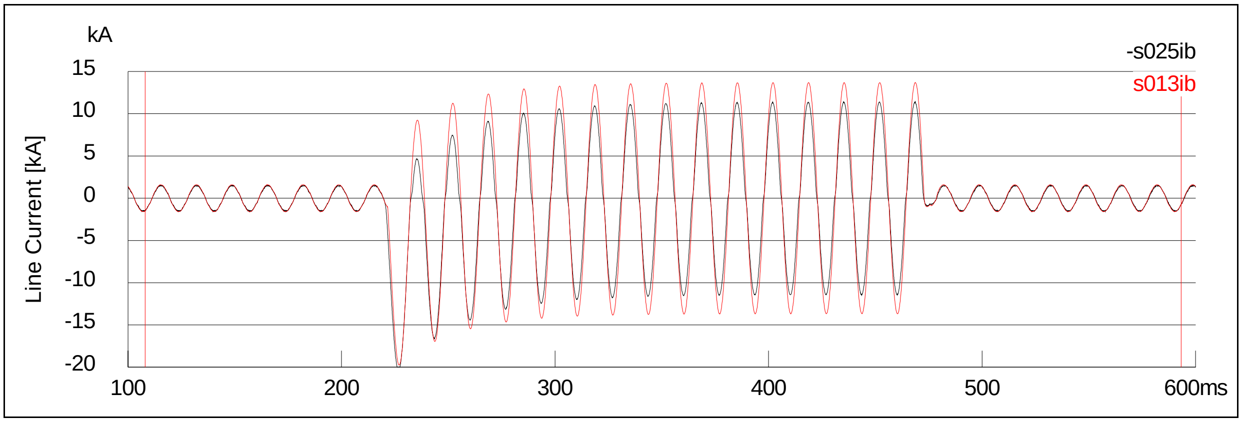

Fig. 23: 10kA Fault current – FCL In vs. Out – phase B

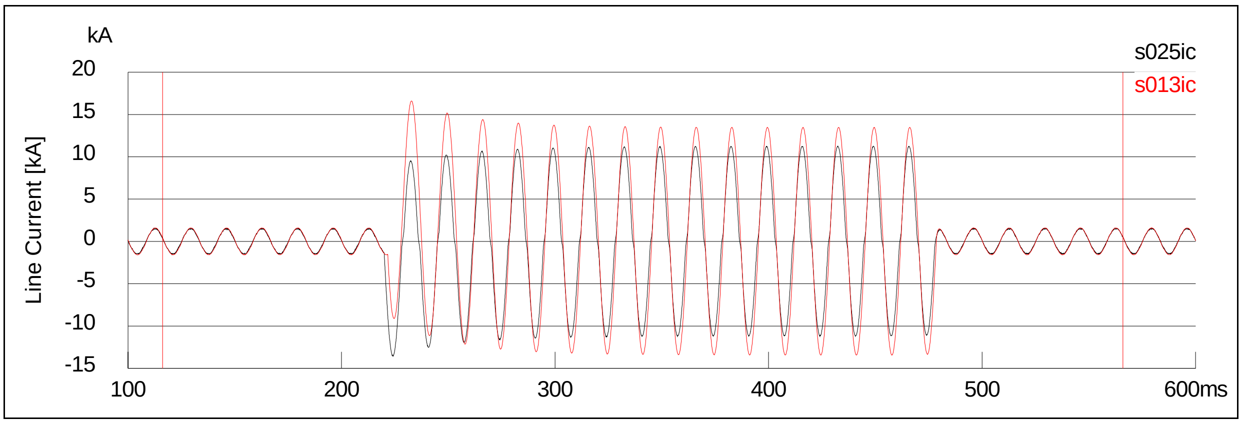

Fig. 24: 10kA Fault current – FCL In vs. Out – phase C

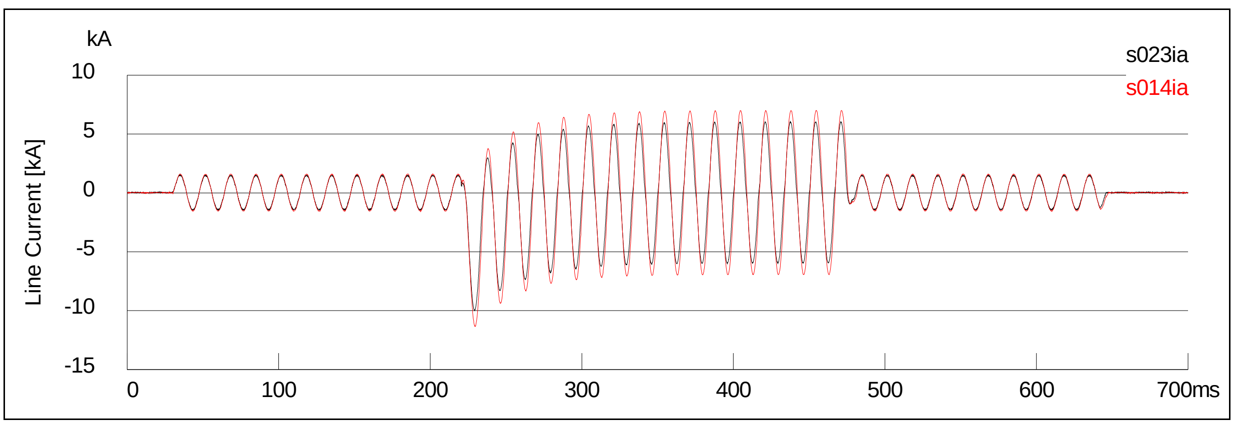

Fig. 25: 5kA Fault current – FCL In vs. Out – phase A

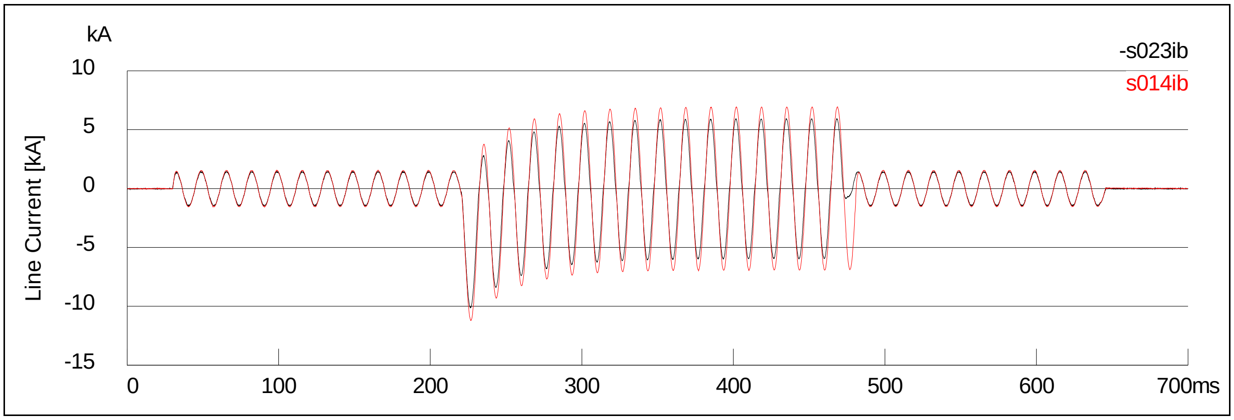

Fig. 26: 5kA Fault current – FCL In vs. Out – phase B

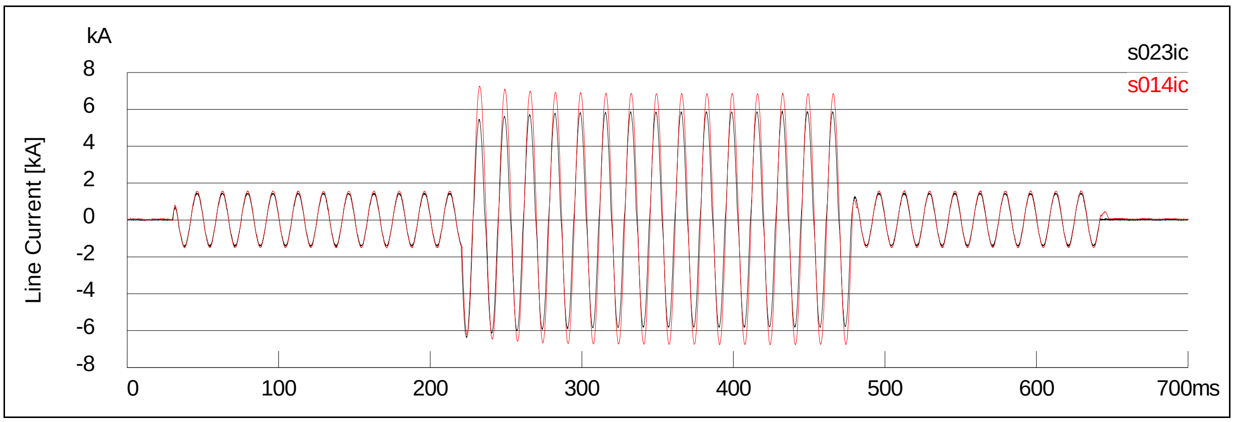

Fig. 27: 5kA Fault current – FCL In vs. Out – phase C

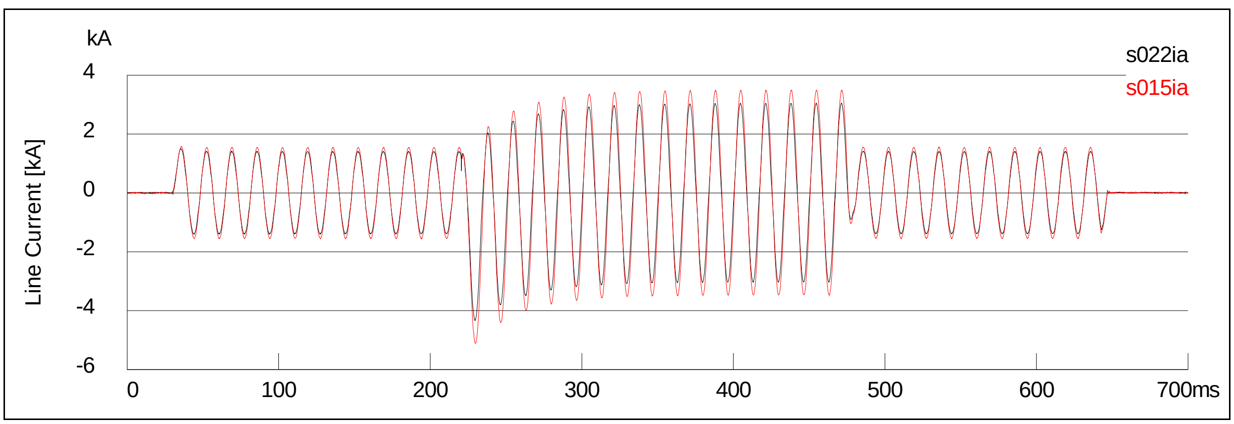

Fig. 28: 2.5kA Fault current – FCL In vs. Out – phase A

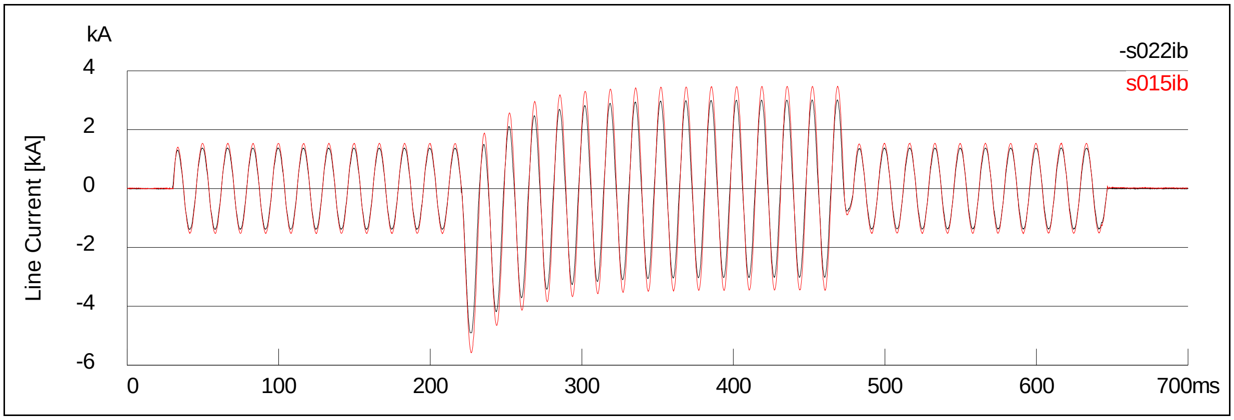

Fig. 29: 2.5kA Fault current – FCL In vs. Out – phase B

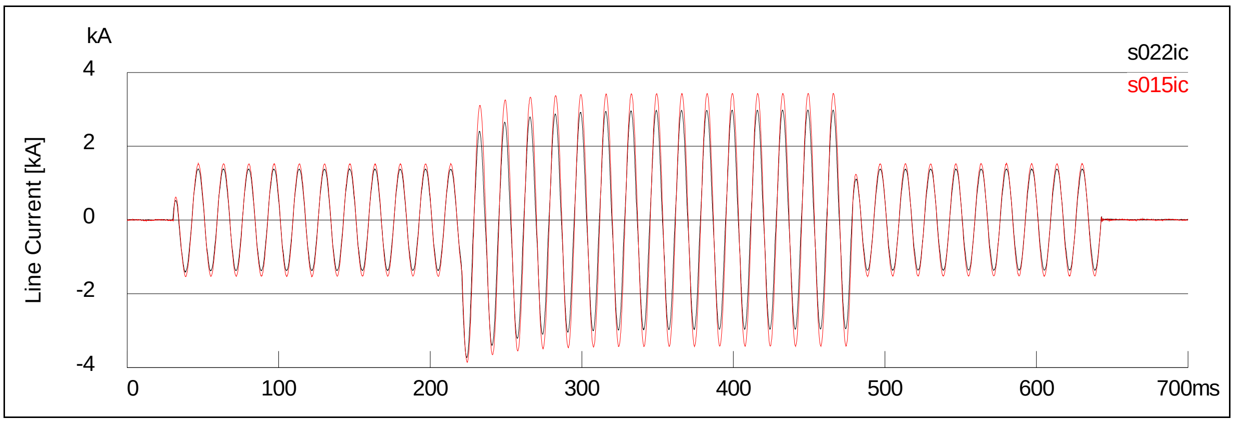

Fig. 30: 2.5kA Fault current – FCL In vs. Out – phase C

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10. Appendix

10.1 FCL Functional testing schedule Rev 01 Nov 27 2007

1. *FCL Test set up*
2. *HTS Coil Cool Down and HTS Coil Testing*
3. *Core Saturation Measurements*
4. *Magnetic flux mapping measurements*
5. *Fault Current Characterization – FCL out of circuit*
6. *Transient Fault Current Limiting – Functional tests – FCL in circuit*
7. *Steady State Conditions – FCL in circuit*
8. *Cryostat Heat losses*
9. *LN2 Temperature Control with increased DC bias current*

1. FCL Test set up

Saturday 8th , Sunday 9th, Monday 10th

SCP is scheduled to arrive on site Saturday morning and spend the weekend and Monday the 10th to set up the FCL and prepare for testing.
LN2 is scheduled to arrive on site Monday morning.

2. HTS Coil Cool Down and HTS Coil Testing

Monday 10th, Tuesday 11th

- Electrical continuity test of DC coil in dry state
- Cool down coil with LN2 according to the recommended Trithor procedure
- Electrical continuity in cooled state
- Detailed current versus voltage diagram of the DC coil to be measured
- Confirm DAQ system hardware and software

3. Core Saturation Measurements

Tuesday 11th

Search coil tests will be performed to measure core flux density as a function of DC current.

4. Magnetic flux mapping

Tuesday 11th

The magnetic field in air around the cryostat and around the FCL structure will be measured with a tri-axis Hall probe. We will establish a map of the magnetic field in air to be compared to FEM results.

5. Fault Current Characterization – FCL out of circuit

Wednesday 12th

The fault current without the FCL in the circuit is measured to confirm the impedance bay and load bay set up.

Error! Reference source not found. shows the impedance set up for the various tests to be scheduled. The first three of these tests will establish the base case fault current waveforms without the FCL in circuit.

FCL status (in circuit or out of circuit)	Secondary Voltage of main Transformer (line to line)	Steady state line current before fault introduced	Load bank Z required	Time duration of steady state current required	Steady state fault current on load side	Source limiting impedance required (nominal)	Time required for fault current to flow	I^2t of fault	Time required for steady state current to flow after fault
	kV rms	A (rms)	Ω	cycles	kA	mΩ	cycles	A^2s (x 10^6)	cycles
Out	13.1	1200	17 Δ	10	2.50	3025	15	3.125	30
Out	13.1	1200	17 Δ	10	5.00	1513	15	12.50	30
Out	13.1	1200	17 Δ	10	10.0	756	15	50.00	30

Table 1. Tests required without the FCL in circuit. Zero voltage crossing on one phase required

6. Transient Fault Current Limiting functional tests – FCL in circuit

Wednesday 12th, Thursday 13th

The FCL is connected into the circuit and the complete set of six tests is repeated under exactly the same conditions. Depending on initial results and analysis further sets of analogous tests may be run with different settings on the FCL tap arrangements and biasing conditions.

FCL status (in circuit or out of circuit)	Secondary Voltage of main Transformer (line to line)	Steady state line current before fault introduced	Load bank Z required	Time duration of steady state current required	Steady state fault current on load side	Source limiting impedance required (nominal)	Time required for fault current to flow	I^2t of fault	Time required for steady state current to flow after fault
	kV rms	A (rms)	Ω	cycles	kA	mΩ	cycles	A^2s (x 10^6)	cycles
In	13.1	7	1100Y	360	2.50	3025	30	1.56	30
In	13.1	7	1100Y	360	5.00	1513	30	6.25	30
In	13.1	7	1100Y	360	10.0	756	30	25.00	30
In	13.1	1200	17 Δ	10	2.50	3025	15	3.125	30
In	13.1	1200	17 Δ	10	5.00	1513	15	12.50	30
In	13.1	1200	17 Δ	10	10.0	756	15	50.00	30

Table 2. Tests required with the FCL in circuit. Nac = 40. Idc = 100. Ndc = 800. Zero voltage crossing on one phase required

7. Steady State Conditions – FCL in circuit

Thursday 13th

Table 3 shows the set of tests required to establish the steady state operational characteristics of the FCL. No fault will be introduced for these tests.

Secondary Voltage of main Transformer bank	Steady state current through FCL required	Load bank Impedance on load side of FCL	Powertech Source limiting impedance required	Time duration of steady state current	I^2t of the steady state current
kV	A	Ω	Ω	s	A^2s (x 10^6)
13.1	200	37.8Y	As required	≤ 5	
13.1	600	12.6Y	As required	≤ 5	
13.1	1200	17 Δ	As required	≤ 5	

Table 2. With FCL in circuit. Steady state functional tests only. Nac = 40. Idc = 100. Ndc = 800.

8. Cryostat Heat losses

Tuesday 11th through Friday 14th

Liquid Nitrogen level will be monitored and logged during testing.
Heat losses will be calculated from LN2 level probe.

9. LN2 Temperature Control with increased DC bias current

Friday 14th

In this final test we will evacuate the space in the LN2 tank in order to decrease pressure and LN2 temperature.
Repeat HTS critical current test at lower temperature.
Run HTS coil at the highest DC current allowable.
Repeat search coil tests to measure core flux density.
If time allows, repeat one steady state condition test and one fault limiting condition test.

FRIDAY 14th – END of TEST

Revisions

Issue	Date	Action	Modified Page
1	12/31/07	First Release	

APPENDIX C:
Zenergy Power HTS FCL Dielectric and HV Test

Test Report

Reporting Center (full name and address):			Zenergy Power Inc. 379 Oyster Point Blvd., Suite 1 South San Francisco, CA USA 94080-1961 Tel.: +1-650-615-5700		
Responsible Person:					
Project Name:	CEC Avanti				
Document Title:	Dielectric and HV Tests 2008				
Document Ref.No.:	**ZP/TR-2008/02**	Reg: #		Page 1	
Date of issue:	11/09/08	Classification:	Confidential	No. of pages:	29
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Author(s):	F. De La Rosa F. Moriconi A. Singh W. Schram	Approved:	F. Moriconi	Order No.:	
Distribution:	A. Kamiab, A. Hood (SCE), K. Smedley, L. Cibulka (CEC), C. Rose (LANL), F. Lambert (NEETRAC), B. Nelson, W. Gibson, A. Rodriguez, S. Ramsay (Zenergy USA), C. Buehrer, J. Keller (Zenergy DE), F. Darmann (Zenergy AUS)				
Distribution page 1:					
Keywords:	FCL dielectric test, FCL impedance, DC resistance, insulation power factor, losses, applied voltage, turn to turn test, BIL, lightning, full wave, chopped wave, partial discharge, PD				

Summary:
Results of tests including dielectric insulation and high voltage tests are presented in this report. These comprise winding DC resistance, impedance, losses, applied voltage and dielectric tests that were conducted at T&R Electric in Colman, South Dakota. High voltage tests conducted at Powertech in Surrey, BC in Canada include turn–to-turn, BIL full lightning and chopped lightning impulse, Partial Discharge and Applied Voltage..

Contents **Page**

1. Test Results Summary

Table 1 summarizes the tests and results on the Avanti circuit FCL.

TEST	Reference Document	RESULTS
Winding Resistance	IEEE Std C57.16-1996	Done
Impedance	IEEE Std C57.16-1996	Done
Total loss	IEEE Std C57.16-1996	Done
Temperature rise	IEEE Std C57.16-1996	Partially done.
Applied voltage	IEEE Std C57.16-1996	Test OK @15 kV
Insulation power factor	IEEE Std C57-12.01-2005	Passed
Insulation resistance measurement	IEEE Std C57-12.01-2005	Done
Fault current tests	Engineering Spec. ZP-ES-08-05	Done
Turn-to-turn	Engineering Spec. ZP-ES-08-05	Passed
Lightning impulse @110 kV	Engineering Spec. ZP-ES-08-05	Passed
Chopped-wave impulse	Engineering Spec. ZP-ES-08-05	Passed (*)
Audible sound	Engineering Spec. ZP-ES-08-05	Not performed
Partial Discharge	Engineering Spec. ZP-ES-08-05	Passed
Applied voltage	IEEE Std C57.16-1996	Passed @ 34 kV
RIV test	Engineering Spec. ZP-ES-08-05	Not performed

(*) Partially only. Phases A and B OK. Phase C showed multiple flashovers

Table 1: FCL Test Summary

2. Applicability

Saturable-core HTS Fault Current Limiter 15kV class, 1200A

3. Applicable documentation

[1] Engineering Specification, ZP-ES-08-05 rev02 Test Protocol for FCL 15kV 1.2kA 3 Phase Use, ZP Internal Report.
[2] Engineering Report, ZP_ER-2008-02 - FCL Insertion Impedance Analysis.
[3] IEEE Std C57.16-1996; IEEE Standard Requirements, Terminology, and Test Code for Dry-Type Air-core Series-Connected Reactors.
[4] IEEE Std C57-12.01-2005: IEEE Standard General Requirements for Dry-Type Distribution and Power Transformers, Including Those with Solid-Cast and/or Resin Encapsulated Windings
[5] NETA's Maintenance Testing Specifications and Acceptance Testing Specifications.
[6] Fault Current Limiter Dielectric Test Report, Powertech Labs Inc., October 2008

4. Acronyms and definitions

4.1 Acronyms

FCL	Fault Current Limiter
HTS	High Temperature Superconductor
CEC	California Energy Commission
BIL	Basic Insulation Level
PD	Partial Discharge

4.2 Definitions

Current Limiting Reactor: A reactor connected in series with the phase conductors for limiting the current that can flow in a circuit under short circuit conditions, or under other operating conditions, such as capacitor switching, motor starting, synchronizing, arc stabilization, etc.

Rating of a Series Reactor: The current that a series reactor can carry at its specified reactance together with any other defining characteristics, such as system voltage, BIL, short circuit current (thermal and mechanical) duty, and frequency.

Rated current: The root mean square (rms) power frequency current in amperes that can be carried for the duty specified, at rated frequency without causing further measurable increase in temperature rise under prescribed conditions of test, and within limitations of established standards.

Short time duty: A requirement of service that requires operation at substantially constant current for a short and definitely specified time.

Nominal voltage: A line to line voltage assigned to a system or circuit of a given voltage class for the purpose of convenient designation.

Rated system voltage: The voltage of a series reactor to which operational and performance characteristics are referred. It corresponds to the nominal line-to-line or phase-to-phase system voltage of the circuit in which the reactor is intended to be used.

Effective resistance (or ac resistance): The value of resistance of a series reactor obtained by dividing the total losses by the current squared at power frequency.

Losses: Those losses are due to current flow. They include:

- The resistance and the eddy-current loss in the winding due to load current
- Losses caused by circulating current in parallel windings
- Stray losses caused by magnetic flux in other metallic parts of the reactor support structure, and in the reactor enclosure when the support structure and the enclosure are supplied as an integral part

of the reactor insulation.

Impedance: The phasor sum of the reactance and resistance, expressed in ohms.

Impedance voltage drop: The product of the rated ohms' impedance and the rated current of a series reactor.

Per unit reactance: On a rated current base, a dimensionless quantity obtained by referencing the magnitude of the reactance to the rated system line-to-neutral voltage divided by the rated current of the reactor. It can also be defined on an arbitrary megavoltampere (MVA) base.

Rated inductance: The total installed inductance at a specified frequency. It may consist of mutual as well as self inductance components.

Rated reactance: The product of a rated inductance and rated angular frequency that provides the required reduction in fault current or other desired modification to power circuit characteristics.

Reactance: The product of the inductance in henries and the angular frequency of the system.

Reactance voltage drop: The component of voltage drop in quadrature with the current.

Resistance voltage drop: the component of voltage drop in phase with the current.

5. General

Dielectric and high voltage tests described in this report were conducted as part of the test plan devised at ZENERGY Power for the Avanti High Temperature Superconductor Fault Current Limiter**.** Test protocols were largely based on the IEEE C57.16-1996 and IEEE C57.12.01-2005 relevant standards, which address testing procedures for Dry-Type Series-Connected Reactors and Dry-type Distribution and Power Transformers including those with Solid Cast and/or Resin-Encapsulated Windings, respectively. These reactors are connected in the power systems to limit fault current under short circuit conditions.

6. Dielectric Insulation Tests

Table 2 summarizes the overall tests described in this report. Tests 1-7 were carried out at T&R Electric in Colman, South Dakota.

#	TEST	Location	Date	Observations
1	Winding Resistance	T&R Electric	9/23/08 to 9/30/08	
2	Impedance	T&R Electric	9/23/08 to 9/30/08	
3	Total loss	T&R Electric	9/23/08 to 9/30/08	
4	Temperature rise	T&R Electric	9/23/08 to 9/30/08	Must be carried out at rated current. Reduced voltage is allowed.
5	Applied voltage	T&R Electric	9/23/08 to 9/30/08	@34kV according to coil manufacturer and IEEE C57.12.01
6	Insulation power factor	T&R Electric	9/23/08 to 9/30/08	
7	Insulation resistance measurement	T&R Electric	9/23/08 to 9/30/08	
8	Turn-to-turn	Powertech	10/20/08 to 10/21/08	
9	Lightning impulse @110 kV	Powertech	10/20/08 to 10/21/08	
10	Chopped-wave impulse	Powertech	10/20/08 to 10/21/08	
12	Partial Discharge	Powertech	10/20/08 to 10/21/08	

Table 2: Avanti FCL Tests

6.1 Winding Resistance measurements

Table 3 shows the DC resistance values found across different sections of the bushing to bushing pathway on the three phases of the FCL during measurements.

WINDING RESISTANCE MEASUREMENT	
Tap/Winding:	DC Resistance
Bushing 1 to Core 1	729 μΩ
Bushing 2 to Core 2	751 μΩ
Bushing 3 to Core 3	759 μΩ
Bushing 4 to Core 4	767 μΩ
Bushing 5 to Core 5	750 μΩ
Bushing 6 to Core 6	769 μΩ
Bushing 1 to Bushing 6	1.604 mΩ
Bushing 2 to Bushing 5	1.644 mΩ
Bushing 3 to Bushing 4	1.636 mΩ

Table 3: FCL AC Winding Resistance Test

6.2 Impedance Measurement

The impedance of the FCL shown in figure 1 was derived from the voltage drop measurements of figure 2 at the load current levels described in table 4. Voltage was measured across the two coils in one of the phases of the FCL. This was done for two different levels of DC bias current, namely 100 A and 140 A on the DC coil, as illustrated in table 4 and figure1.

Source side avg. current (A)	Load side voltage (Vrms)	V drop across FCL (Vrms) Idc= 100A	% V.D. for Idc bias =100A	FCL impedance for Idc=100A (ohms)	V drop across FCL (Vrms) Idc= 140A	% V.D. for Idc bias =140A	FCL impedance for Idc=140A (ohms)
106.1	239.4	5.4	0.07	0.05	5.5	0.08	0.05
213.9	241.3	11.1	0.15	0.05	11.0	0.15	0.05
309.5	243.2	16.2	0.23	0.05	16.2	0.23	0.05
407.5	239.1	22.0	0.31	0.05	21.4	0.30	0.05
509.0	238.5	29.2	0.41	0.06	28.7	0.40	0.06
613.2	239	38.0	0.53	0.06	36.3	0.50	0.06
720.7	241.5	49.7	0.69	0.07	46.0	0.64	0.06
826.0	241	65.8	0.91	0.08	56.4	0.78	0.07
920.1	240	88.3	1.23	0.10	72.8	1.01	0.08
1012.9	240	116.7	1.62	0.12	98.4	1.37	0.10
1125.8	241	159.4	2.21	0.14	n/a	n/a	n/a

Table 4: FCL Impedance Measurement Test Results

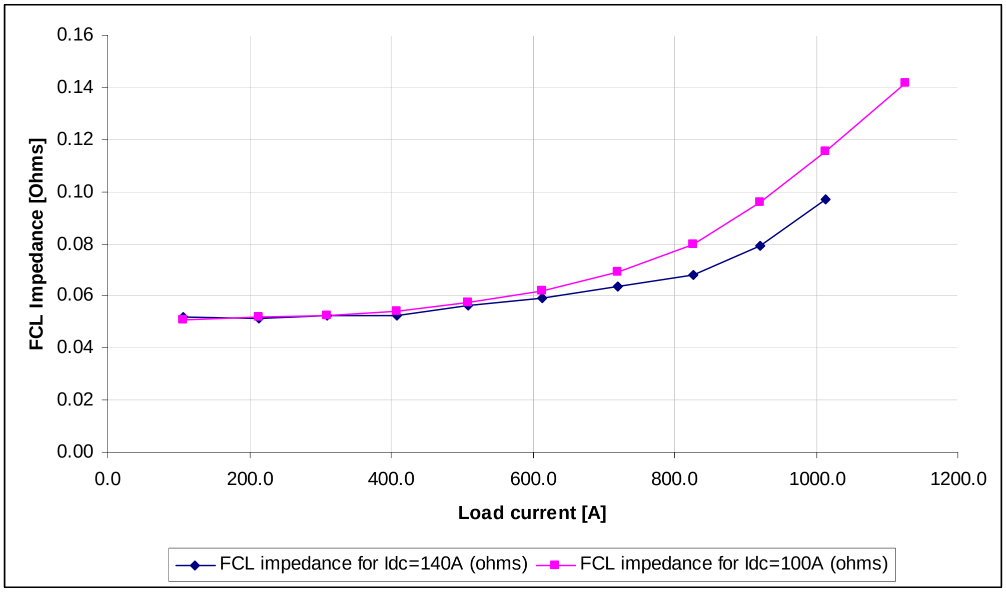


Figure1: FCL Ohmic Impedance Measurement

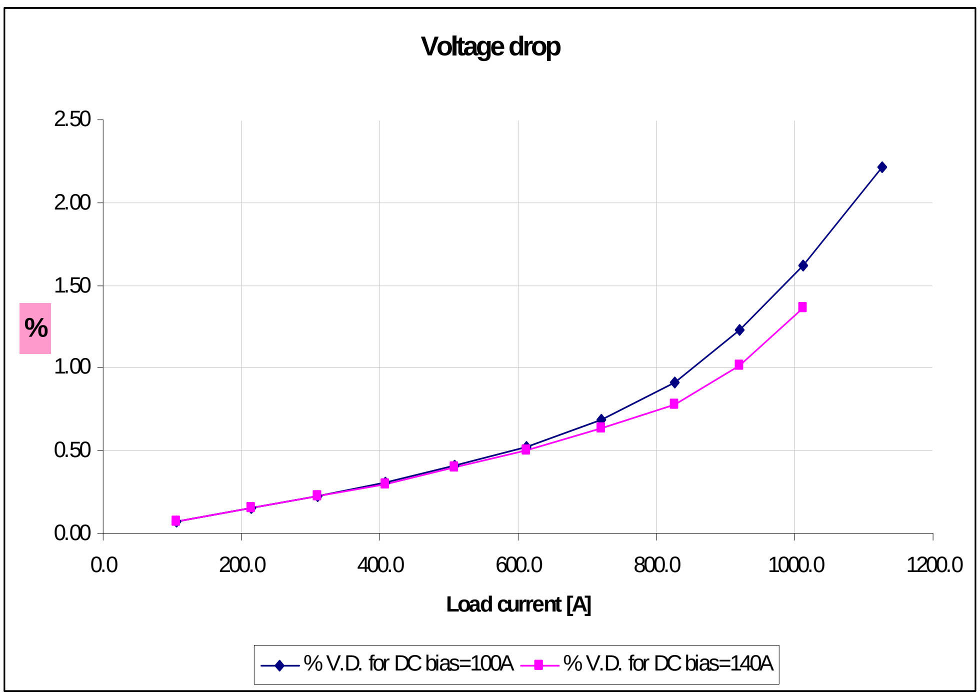


Figure 2: Voltage Drop on FCL for Different Load Currents

6.3 FCL Resistive Loss Measurement

Table 5 and figure 3 depict the losses as a function of load current up to 1100 A, which is the maximum test current used during the test. The resistance used for loss calculations was the bushing to bushing DC resistance. The current applied to the HTS coil during this test was 100 A.

Source side avg. current (A)	Measured Power at Source side [kW]	Apparent Power at source side [kVA]	Load Power factor	Avg. Bushing to Bushing DC Resistance (Ohms)	FCL Calculated Resistive Loss (kW)	FCL Losses %
106.1	44.95	45.10	1.00	0.00163	0.055	**0.12**
213.9	91.59	92.09	0.99	0.00163	0.224	**0.24**
309.5	133.60	134.87	0.99	0.00163	0.468	**0.35**
407.5	173.28	176.03	0.98	0.00163	0.811	**0.47**
509.0	216.93	222.63	0.97	0.00163	1.265	**0.58**
613.2	264.54	275.33	0.96	0.00163	1.836	**0.69**
720.7	312.07	332.90	0.94	0.00163	2.537	**0.81**
826.0	358.50	395.15	0.91	0.00163	3.332	**0.93**
920.1	397.62	460.78	0.86	0.00163	4.135	**1.04**
1012.9	441.85	547.28	0.81	0.00163	5.011	**1.13**
1125.8	495.77	683.11	0.73	0.00163	6.190	**1.25**

Table 5: FCL Resistive Losses Results

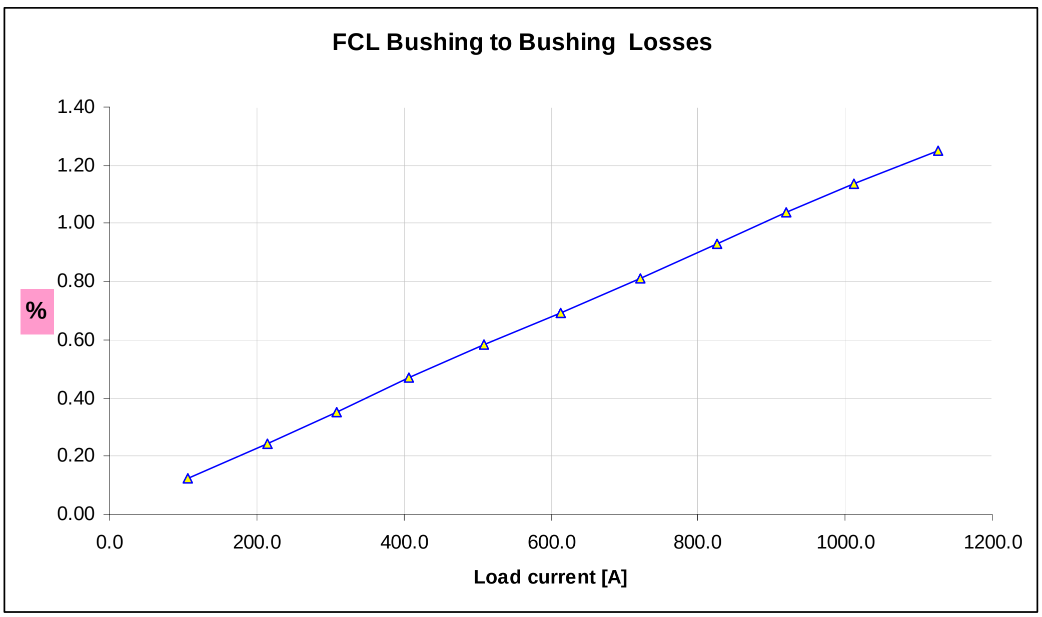


Figure 3: FCL Losses for Different Load Currents

6.4 FCL Temperature Rise Test

Figure 4 depicts the result of the temperature rise test. This test was carried out at 1000 A during a period of over three hours. Temperature was measured at different points on one of the AC coils using thermocouples. The temperature on the AC coil showed the expected increase but the test could not be run long enough to show the expected decrease in rate of rise of temperature required by IEEE C57.16 -1995 (2.5% or 1^{o}C during a period of two consecutive hours).

A collection of thermal images of different parts of the FCL during this test is presented in the Appendix. Zenergy Power will conduct a second test at reduced voltage to try getting to the point where temperature rise decreases at the rate established in IEEE C57.16-1995.

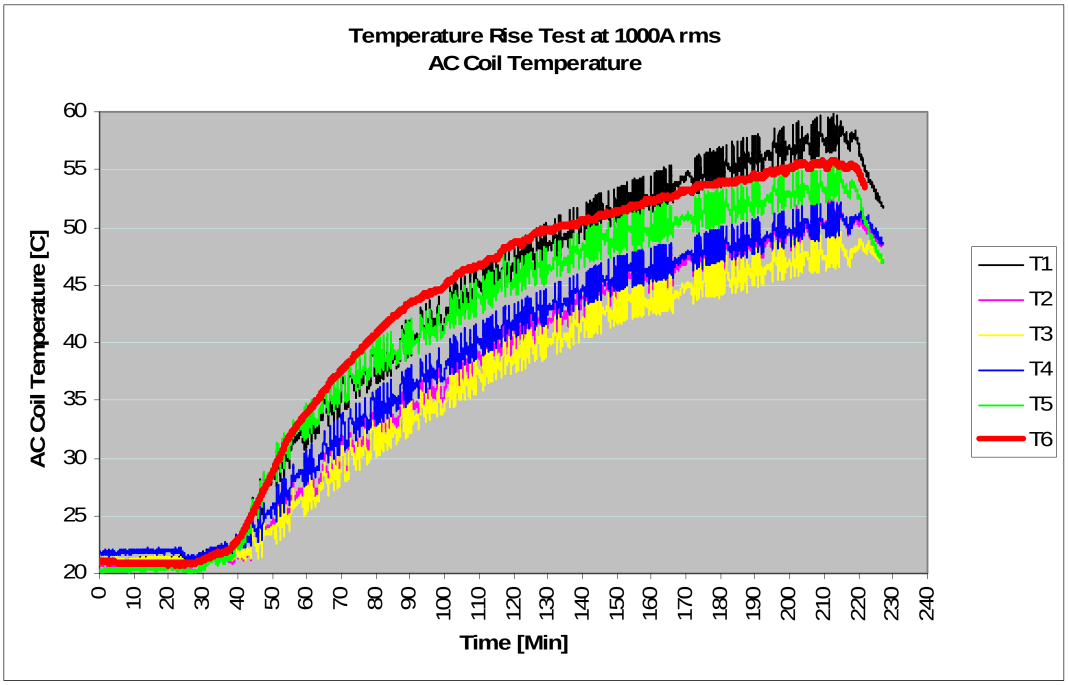


Figure 4. AC Coil Temperature Measured During the Temperature Rise Test

6.5 FCL Applied Voltage Test

Due to lack of proper cable terminations to connect onto the bushings of the FCL, applied voltage test at T&R was limited to only 15 kV, which was well endured by the FCL but the test felt short of the 34 kV voltage required by IEEE C57.12.01 for a 15 kV device. This test was successfully repeated at Powertech with the required voltage applied for 60 seconds.

6.6 FCL Insulation Power Factor

This test most indicative of voids in the coil insulation involves measurement of the ratio between capacitance and resistance leakage within the coil insulation material. This test was conducted and yielded the results described in table 6. The measured resistance value of around 1.6 mΩ in table 5 is insignificant compared with the capacitive reactance (around 2.666 MΩ) derived from the measured capacitance in table 5. This yields a near 90 degrees angle, for which the resultant insulation power factor would be well below the 0.5% recommended value in IEEE C57.12.01 [4]

ID	kV	Cap(pF)	mA @ 2.5kV	W @ 2.5kV	mA @ 10kV	W @ 10kV
A TO GRD	10	935.14	0.895	0.393	3.58	6.289
B TO GRD	10	1109.4	1.062	0.47	4.248	7.52
C TO GRD	10	942.16	0.9	0.3805	3.603	6.088

Table 6: FCL Insulation Power Factor Test

6.7 Insulation Resistance Measurement

This test was performed to test the integrity of the insulation of the AC coils. Insulation resistance measurements were carried out on the FCL per IEEE C57.12.101-2005 yielding the results described in table 7. The insulation levels found are above the 5000 MΩ level recommended by NETA [5]. The lower level for insulation between phases A and B may be due to LV signal cables from the TP's and TC's that were in contact with the power conductors as they passed through the same opening on the dividing wall between the compartments. Another possibility is the proximity of the taps to one of the supporting blocks in one of the coils, where sparkover activity during impulse testing consistently occurred.

Test applied between phases:	A-B	A-C	B-C
Measured Insulation Resistance Value (MΩ)	54,600	954,000	974,000

Table 7: FCL AC Winding Resistance Test

7. HIGH VOLTAGE TESTS

Tests 8-12 in table 2 were carried out at Powertech Lab in Surrey, BC in Canada. This report summarizes the results of HV testing described in the Powertech Test Report [6].

7.1 Partial Discharge Test

The load and source terminals of each phase of the fault current limiter were connected together. Each phase was energized at a pre-stress level of 11.3 kV L-G for 10 seconds. The voltage was then reduced to 9.5 kV, held for 60 seconds and then the partial discharge was measured. After the first partial discharge test each phase was energized at the applied potential test level of 34 kV for 60 seconds. The voltage was then reduced to 9.5 kV [i.e $(15/\sqrt{3})*1.1$, or 110% of rated L-G voltage], held for 60 seconds and then the partial discharge level was measured again. As illustrated in table 8, partial discharge levels at 9.5 kV fell below the recommended 100 pC value in the three phases.

Phase	Voltage (kV)	Partial Discharge (pC)	Remarks
A	11.23 kV Pre-stress 10 sec	>400	Original condition
A	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	>400	Original condition
A	11.23 kV Pre-stress 10 sec	80	After modifying cables and CT's arrangement
A	9.5 kV Measurement Level (Limit < 100 pC)	58	After modifying the cables and CT's arrangement
B	11.23 kV Pre-stress 10 sec	>400	Original condition
B	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	>400	Original condition
B	11.23 kV Pre-stress 10 sec	36	After modifying the cables and CT's arrangement
B	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	16	After modifying the coil to coil cable and CT's arrangement
C	11.23 kV Pre-stress 10 sec	321	After modifying the cables and CT's arrangement
C	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	28	After modifying the cables and CT's arrangement

Table 8: Partial Discharge Test data

7.2 Lightning Full Impulse test

A lightning impulse test was carried out on each phase of the fault current limiter with the source and load terminals of the phase under test connected together. Each phase was subjected to one reduced full wave and three full waves of positive polarity, as illustrated in table 9, with a crest voltage of 110 kV for the full waves. Figure 5 illustrates examples of the measured lightning impulse waveforms.

The FCL initially failed the full wave lightning impulse tests due to flashovers created from the high voltage leads to grounded points. After re-arranging the leads all three phases withstood the lightning impulse tests.

Winding		A phase reactor winding	B phase reactor winding	C phase reactor winding
Rated voltage		15 kV	15 kV	15 kV
Test Voltage	full wave	110 kV	110 kV	110 kV
Polarity		positive	positive	positive
Terminals tested		Load & source terminals connected together	Load & source terminals connected together	Load & source terminals connected together

Table 9: Full Wave Lightning Impulse Test data

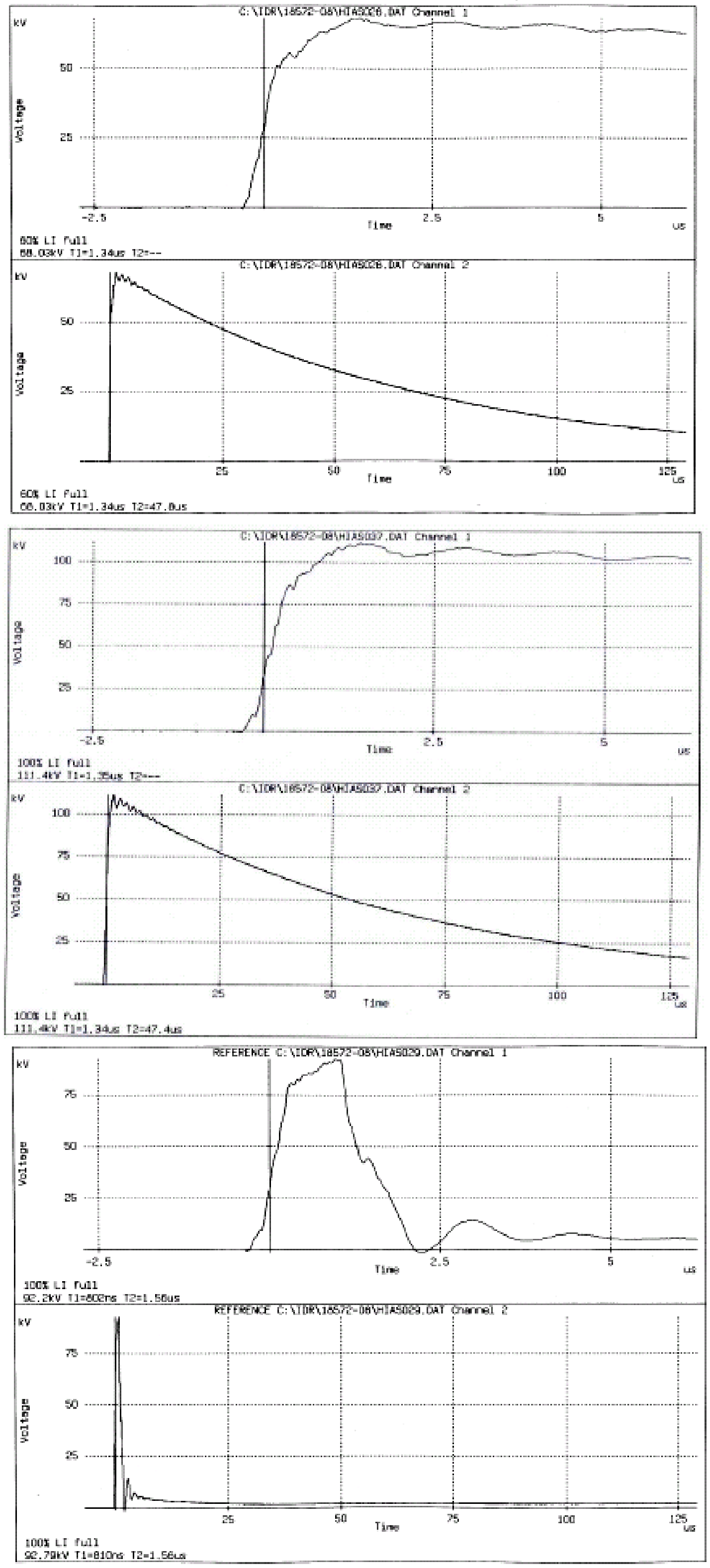


Figure 5: Full Wave Lightning Impulse Test Waveforms

7.3 Chopped Wave Impulse test

A chopped wave impulse test was carried out on each phase of the fault current limiter with the source and load terminals of the phase under test connected together. As depicted in table 10, each phase was subjected to one reduced full wave, one full wave, one reduced chopped wave, two chopped waves, followed by two full waves, with a crest voltage of 110 kV for the full waves and 120 kV for the chopped waves. Figure 6 gives examples of the applied chopped impulse waveforms.

The FCL initially had flashovers on the chopped impulse and full wave lightning impulses. After re-arranging the leads A and B phases withstood the required series of impulse waves. C phase failed to withstand the closing test sequence of two full lightning impulse waves.

Winding		A phase reactor winding	B phase reactor winding	C phase reactor winding
Rated voltage		15 kV	15 kV	15 kV
Test Voltage	full wave	110 kV	110 kV	110 kV
Test Voltage	Chopped wave	120 kV	120 kV	120 kV
Polarity		positive	positive	positive
Terminals tested		Load & source terminals connected together	Load & source terminals connected together	Load & source terminals connected together

Table 10: Chopped Lightning Impulse Test data

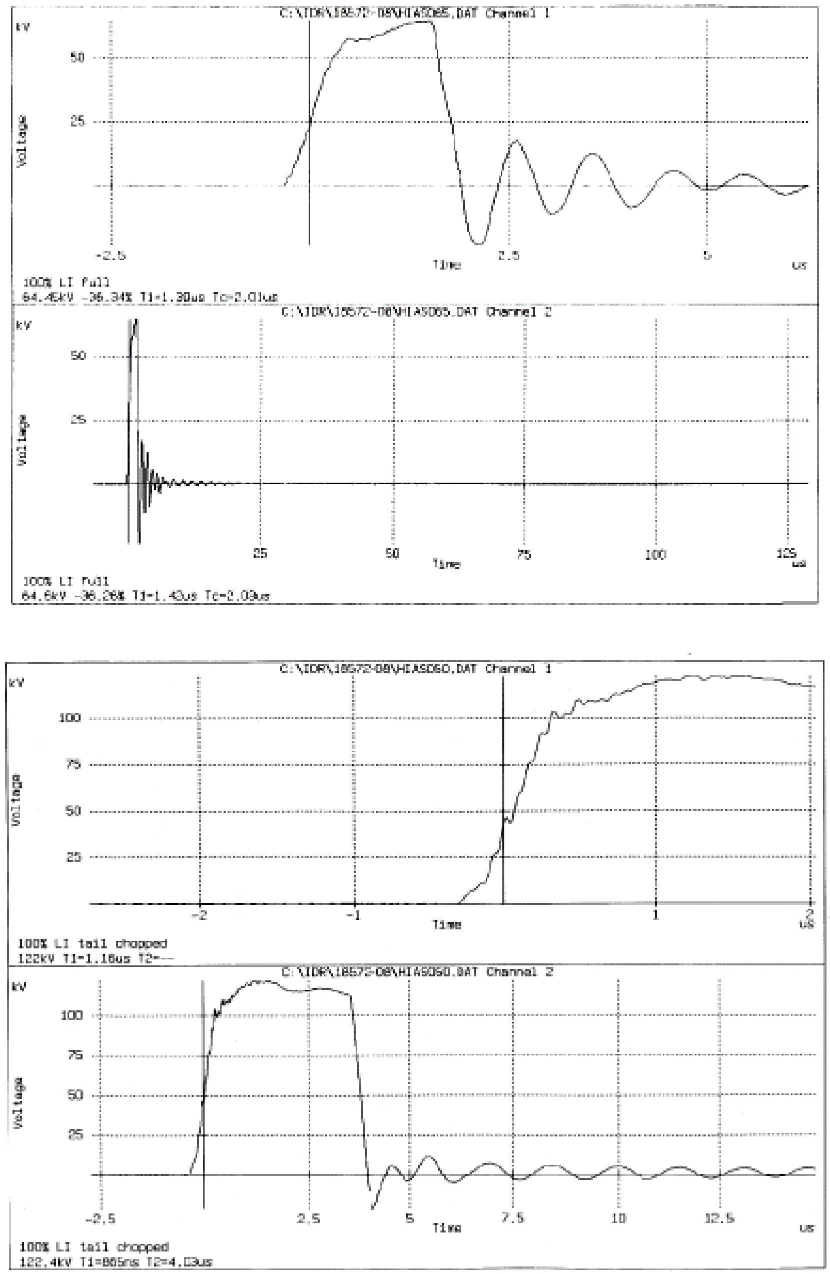


Figure 6: Chopped Wave Lightning Impulse Test Waveforms

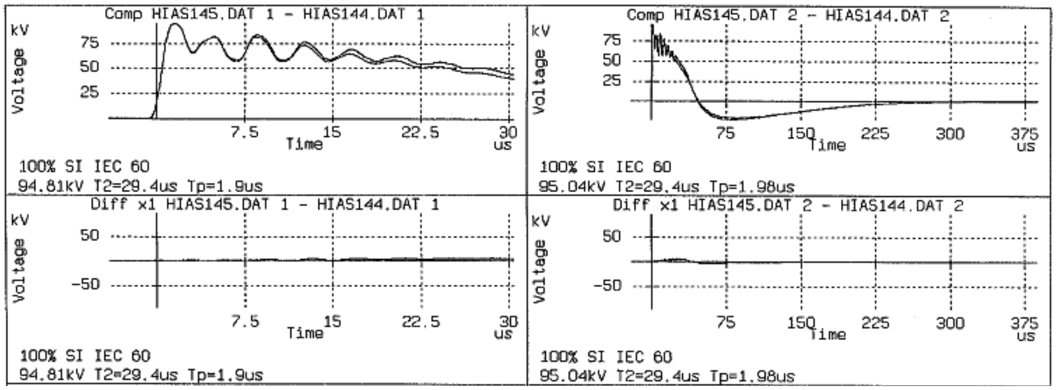
7.4 Turn to Turn Test

As described in table 11, the turn-to-turn test was done by applying one reduced and three full wave ringing impulse waveforms of positive polarity to each terminal of the fault current limiter. The un-energized terminals of the fault current limiter were grounded during the tests. The peak of the full waveform was 95 kV. Figure 7 gives an example of the applied waveform.

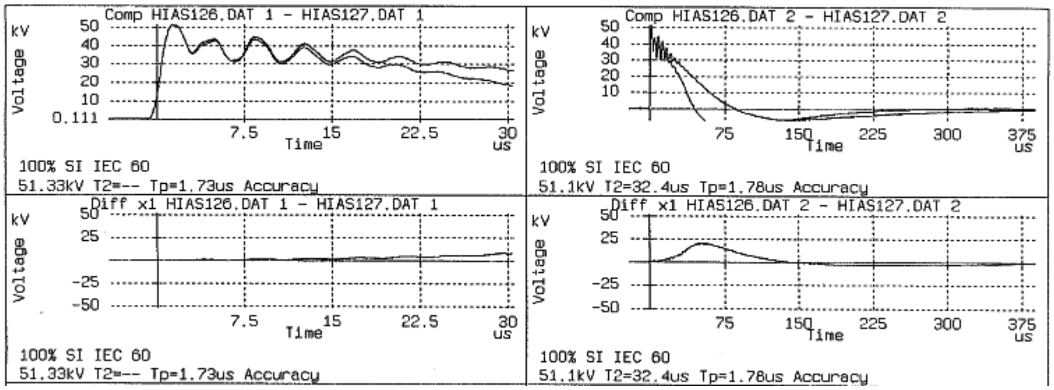
No shift in frequency or damping of the oscillatory pattern between reference voltages was observed during the tests. This indicates that no inter-turn flashover occurred.

Winding		A phase reactor winding	B phase reactor winding	C phase reactor winding
Rated voltage		15 kV	15 kV	15 kV
Test Voltage	Ring wave	95 kV	95 kV	95kV
Polarity		positive	positive	positive
Terminals tested		HV: Load terminal Ground: Source terminal	HV: Load terminal Ground: Source terminal	HV: Load terminal Ground: Source terminal
Terminals tested		HV: Source terminal Ground: Load terminal	HV-Source terminal Ground-Load terminal	HV: Source terminal Ground: Load terminal

Table11: Turn-to-Turn Ringing Wave Test data



a) Turn-to-turn A Ø Load Side (Both Waves 95.8 kV)



b) Turn-to-turn B Ø Load Side (Full – 97.6 kV, Reduced – 51.3 kV)

Figure 7. Turn to Turn Test Waveforms

7.5 Applied Voltage test

After the first partial discharge test each phase was energized at the applied potential test level of 34 kV for 60 seconds. As illustrated in table 12, the voltage was then reduced to 9.5 kV, held for 60 seconds and then the partial discharge was measured again. The FCL successfully withstood the applied voltage in the three phases.

Phase	Voltage (kV)	Partial Discharge (pC)	Remarks
A	11.23 kV Pre-stress 10 sec	>400	-
A	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	23	-
A	34 kV Applied voltage 1 min	withstood	-
A	9.5 kV Measurement Level (Limit < 100 pC)	60	-
B	11.23 kV Pre-stress 10 sec	48	-
B	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	12	-
B	34 kV Applied voltage 1 min	withstood	-
B	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	11	-
C	11.23 kV Pre-stress 10 sec	117	-
C	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	22	-
C	34 kV Applied voltage 1 min	withstood	-
C	9.5 kV Measurement Level Held for 1 min (Limit < 100 pC)	22	-

Table12: Applied Voltage Test data

Conclusions

Dielectric and High Voltage Testing of the Zenergy Power FCL performed at T&R Electric in South Dakota and Powertech in Surrey, B.C. revealed an overall solid performance of the Avanti FCL but also showed the need to perform some additional enhancement work on the jumper cable and cable terminations connecting to the AC coils. The load side coil on phase C showed persistent flashovers during impulse testing apparently initiated at on one of the coil taps and tracking over a supporting dielectric block that was found to be inconveniently close to to the taps. This coil is to be rotated to increase the standoff to prevent impulse flashover. All live exposed parts will be insulated to avoid that corona discharges are initiated at sharp edges.

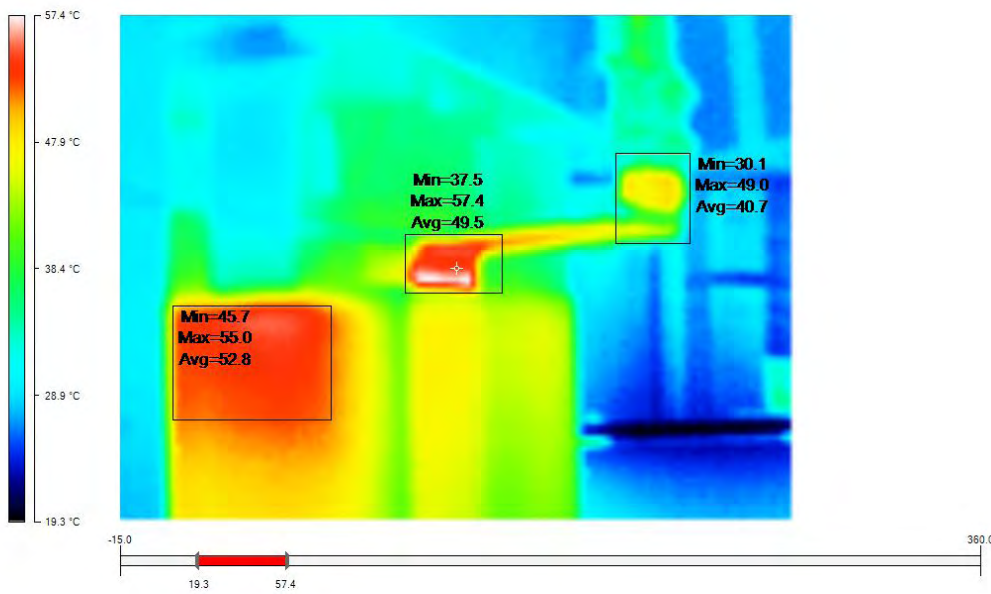
8. List of Tables and Figures

List of Revisions

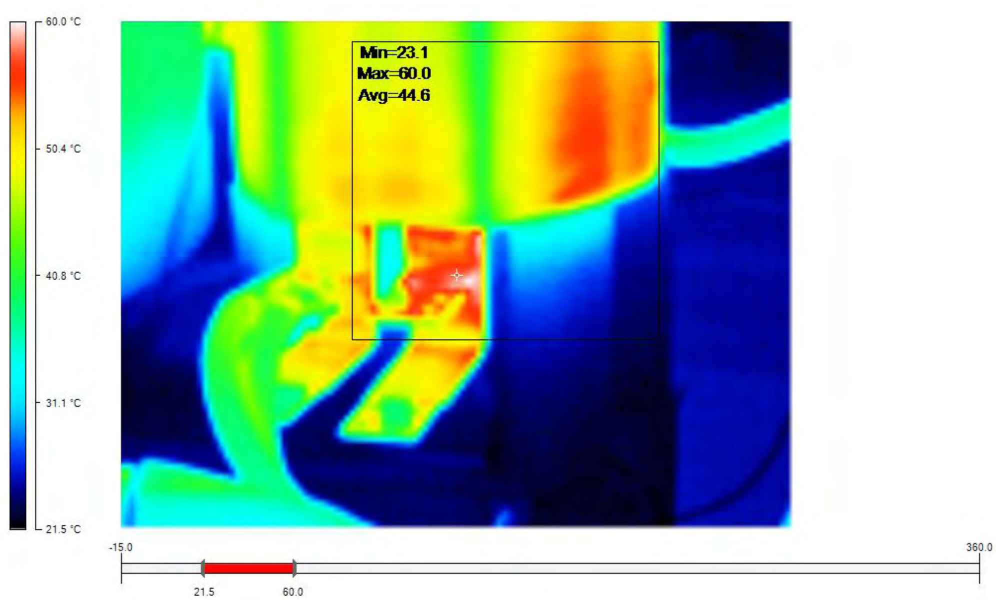
Revision	Date	Action	Modified Page
1	11/09/08	Draft Released	
1	12/03/08	Released	Page 1

9. APPENDIX

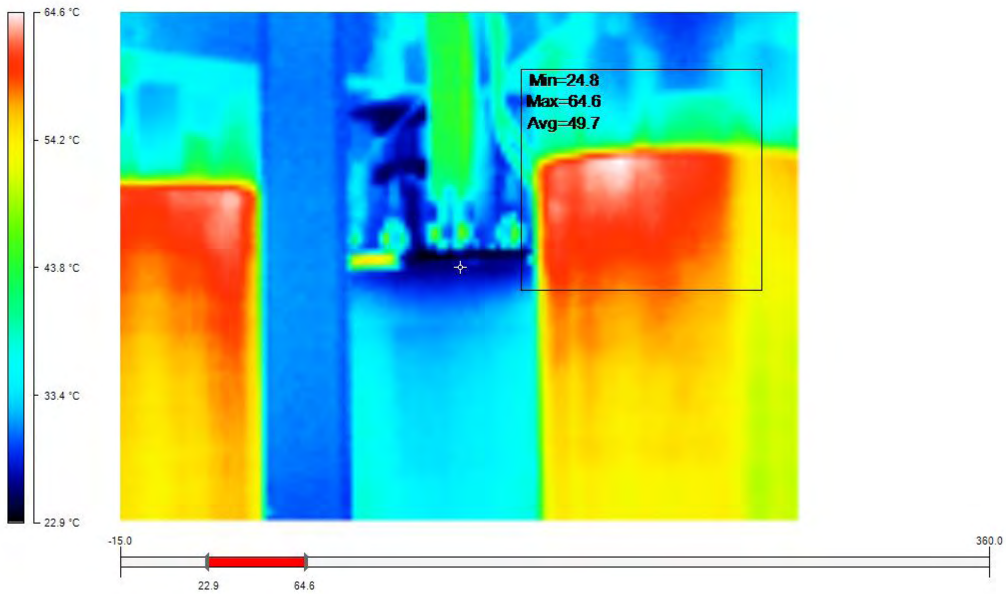
9.1 THERMAL INMAGES OF THE FCL DURING TEMPERATURE RISE TEST AT T&R



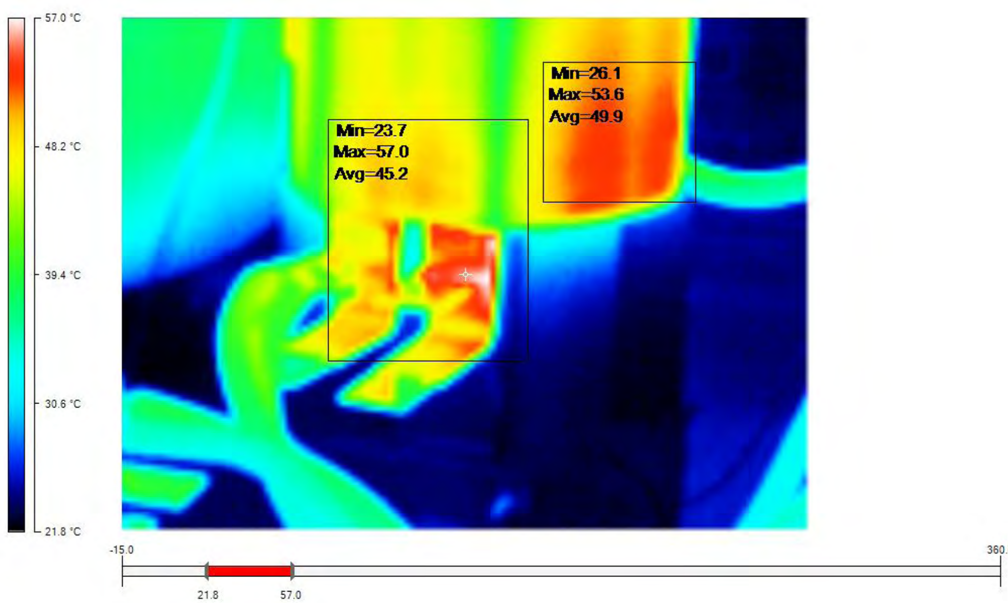
AC COIL TEMPERATURE



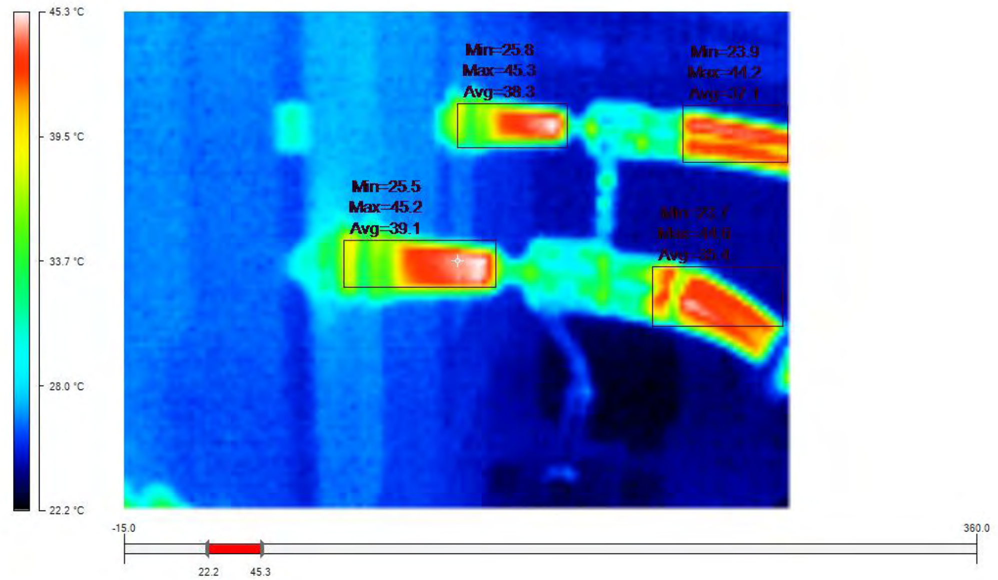
AC COIL TEMPERATURE
60^{o}c



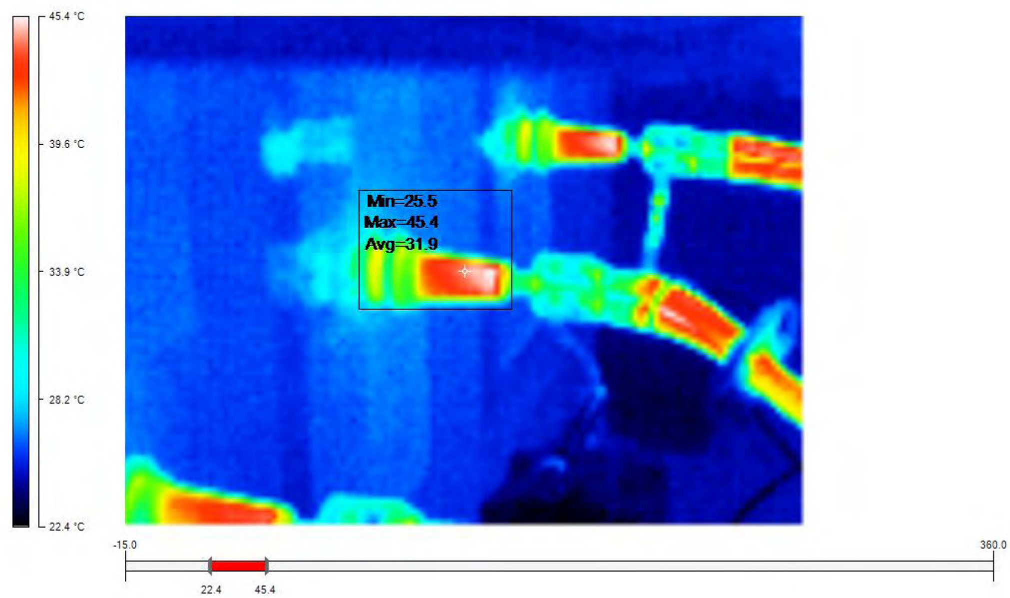
AC_coil_temp_65C



AC_coil_temp_bottom phA



bushing_load-side_01



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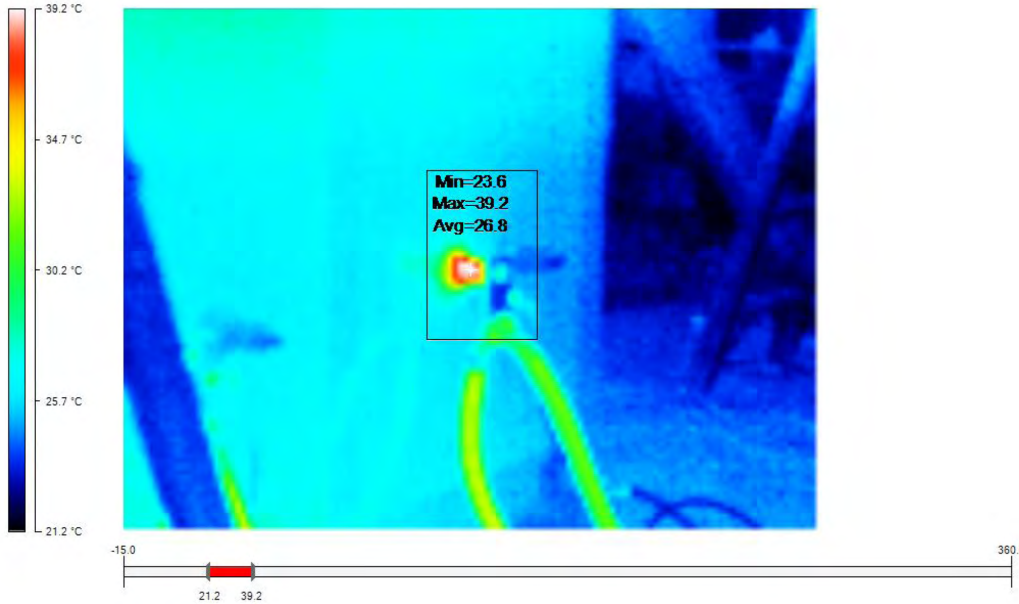
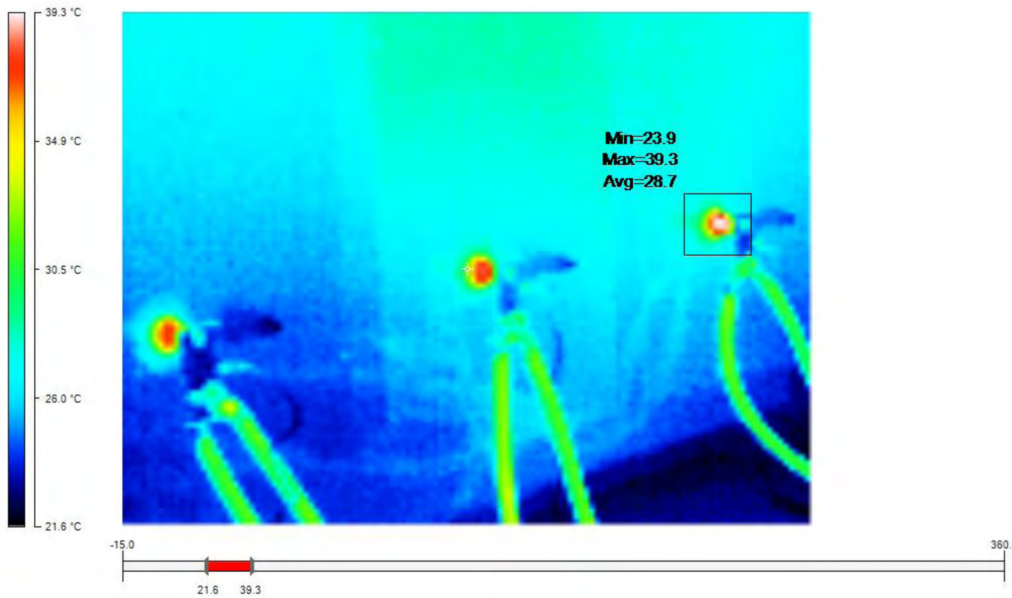


bushing_source-side_01



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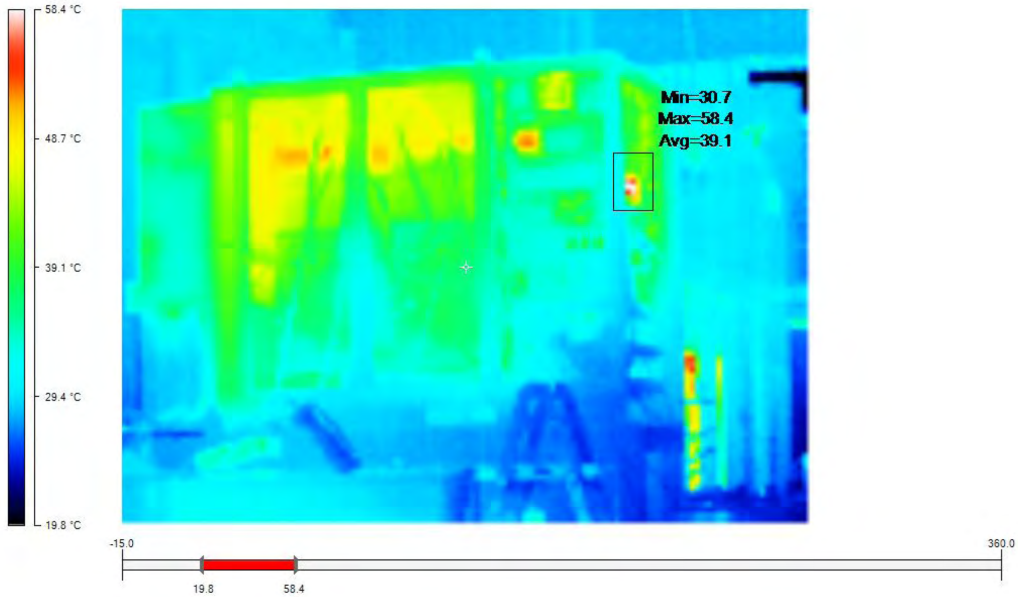

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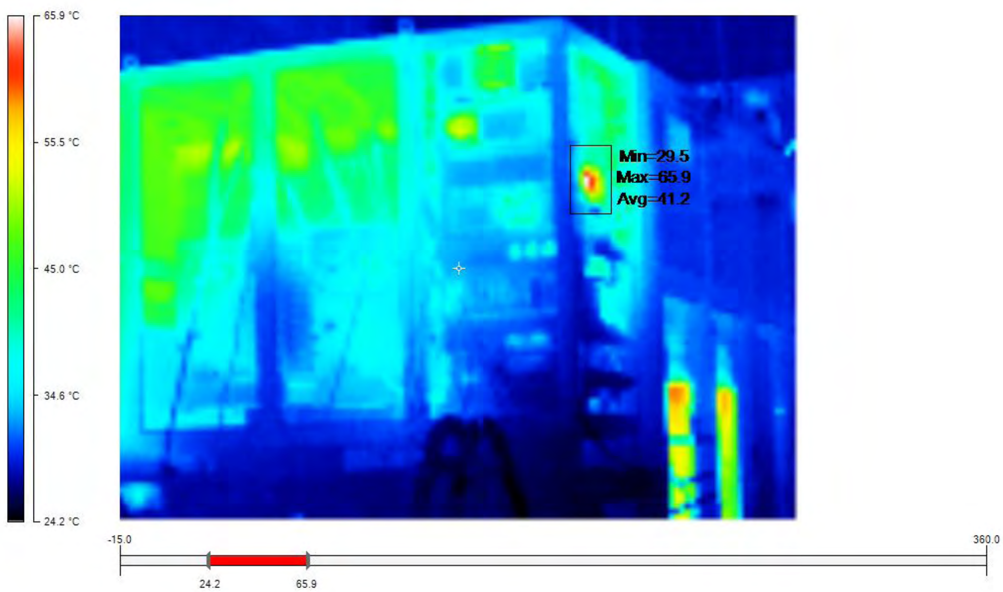
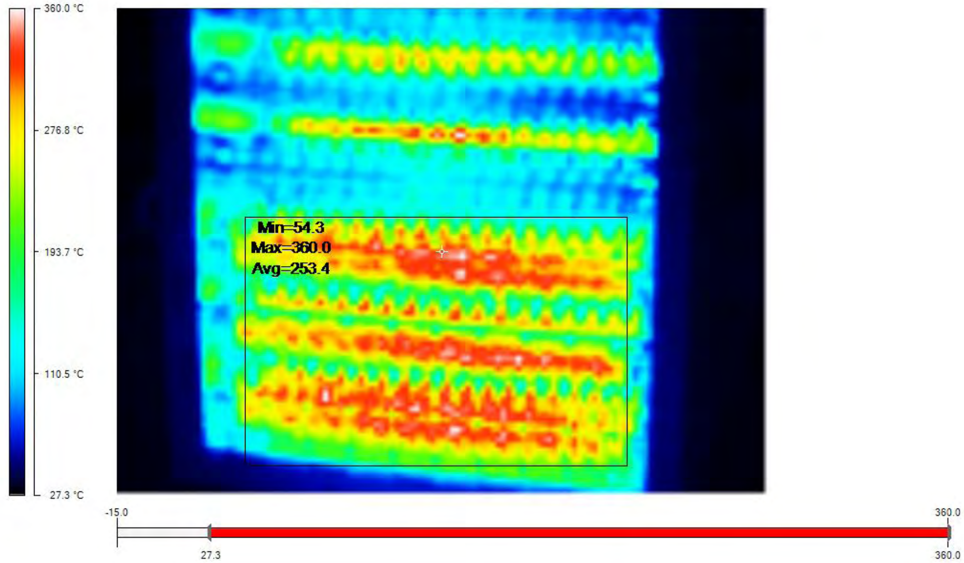
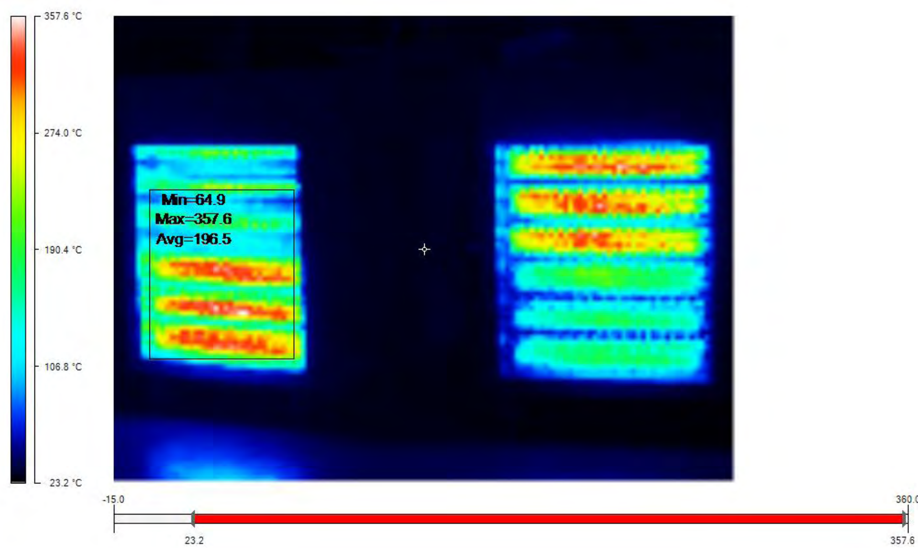


FCL_full_66Cmax



Load-bank



Load-bank_full

APPENDIX D:
Zenergy Power HTS FCL Normal State Temperature Rise Test

Test Report

Reporting Center (full name and address):			Zenergy Power Inc. 379 Oyster Point Blvd., Suite 1 South San Francisco, CA USA 94080-1961 Tel.: +1-650-615-5700		
Responsible Person:	Franco Moriconi				
Project Name:	CEC Avanti				
Document Title:	**Temperature Rise Test**				
Document Ref.No.:	**ZP/TR-2008/03**	Reg: #		Page 1	
Date of issue:	11/30/08	Classification:	Confidential	No. of pages:	19
Client(s):	CEC/SCE				
Author(s):	F. Moriconi F. De La Rosa A. Singh W. Schram	Approved:	F. Moriconi	Order No.:	
Distribution:	A. Kamiab (SCE), Alan Hood (SCE), K. Smedley (CEC UC Irvine), F. Moriconi, W. Schram, R. Lombaerde, A. Singh, M. Levitskaya, F. De La Rosa, A. Singh (ZP USA)				
Distribution page 1:	B. Nelson, W. Gibson, A. Rodriguez, S. Ramsay (ZP USA), F. Darmann (ZP AUS), C. Buehrer (ZP DE)				
Keywords:	Fault Current Limiter, Temperature rise, heat-run				

Summary:
This report presents the results of the temperature rise test on the Avanti circuit Fault Current Limiter carried out at Zenergy Power in South San Francisco, CA, in compliance with the relevant IEEE standard C57.12.01-2005 and under request of Southern California Edison.

Contents **Page**

1. Applicability

Saturable-core HTS Fault Current Limiter 15kV class, 750A.

2. Documentation

[1] CEC Avanti Test Plan for Additional FCL Testing, Zenergy Power Internal Report ZP_ER_2008_06, Dec. 2008.
[2] Engineering Specification, ZP-ES-08-05 rev02 Test Protocol for FCL 15kV 1.2kA 3 Phase Use, ZP Internal Report.
[3] IEEE Std C57.16-1996; IEEE Standard Requirements, Terminology, and Test Code for Dry-Type Air-core Series-Connected Reactors.
[4] IEEE Std C57-12.01-2005: IEEE Standard General Requirements for Dry-Type Distribution and Power Transformers, Including Those with Solid-Cast and/or Resin Encapsulated Windings

3. Acronyms and definitions

3.1 Acronyms

FCL	Fault Current Limiter
HTS	High Temperature Superconductor
CEC	California Energy Commission
SCE	Southern California Edison

3.2 Definitions

Ambient temperature: this is the temperature of the air surrounding the FCL. For the purposes of IEEE Std C57.16-1996, it is assumed that the temperature of the cooling air (ambient temperature) does not exceed 40 ^{o} C and the average temperature of the cooling air for any 24 hour period does not exceed 30 ^{o} C.

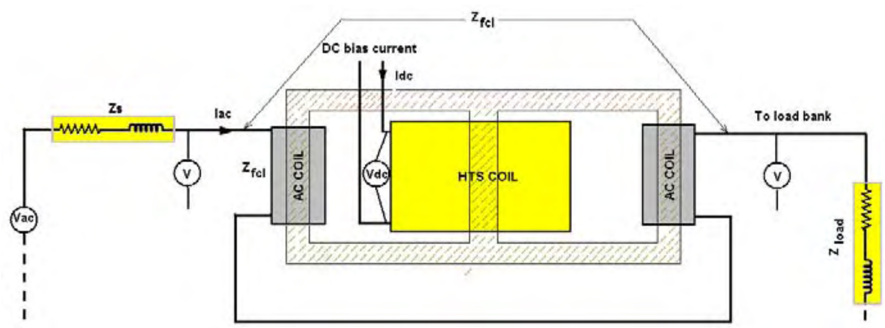
4. General

We successfully measured all HTS and cryostat losses: standby, DC, and induced AC. The FCL was energized with 100A DC bias and 750A AC current 3-phase 60Hz. All measurements were taken at atmospheric pressure and a cryostat temperature of 77K.

The cryostat was filled up to 65-70 cm and losses were estimated by measuring the LN2 boil off rate via a calibrated N2 flow meter

5. Temperature rise test results

The temperature rise test was conducted per test protocol document [1] according to the test setup in figure 1. Temperature was measured on the AC coils with thermocouples on different parts of the AC coils. AC current at 240 V AC from the generator was increased until nominal (750 A) current was reached. The load consisted of resistive load that could be switched on in steps of 5, 10, 25, 50 and 100 kW. Some adjustment on the generator output was applied to compensate for the voltage drop on the FCL.



Vac	=	AC voltage 240 V
Iac	=	Line Current in steps up to 750 A
Idc	=	DC bias current on HTS coil 100 A
Zs	=	Source Impedance, Ω
Zfcl	=	FCL Impedance, Ω
Zload	=	Load Impedance, Ω

Figure 1: Single-phase view schematic of test setup for temperature rise test on Fault Current Limiter

Plots in figures 2-4 show the recorded data for two consecutive run-up and run-down at 750A AC.

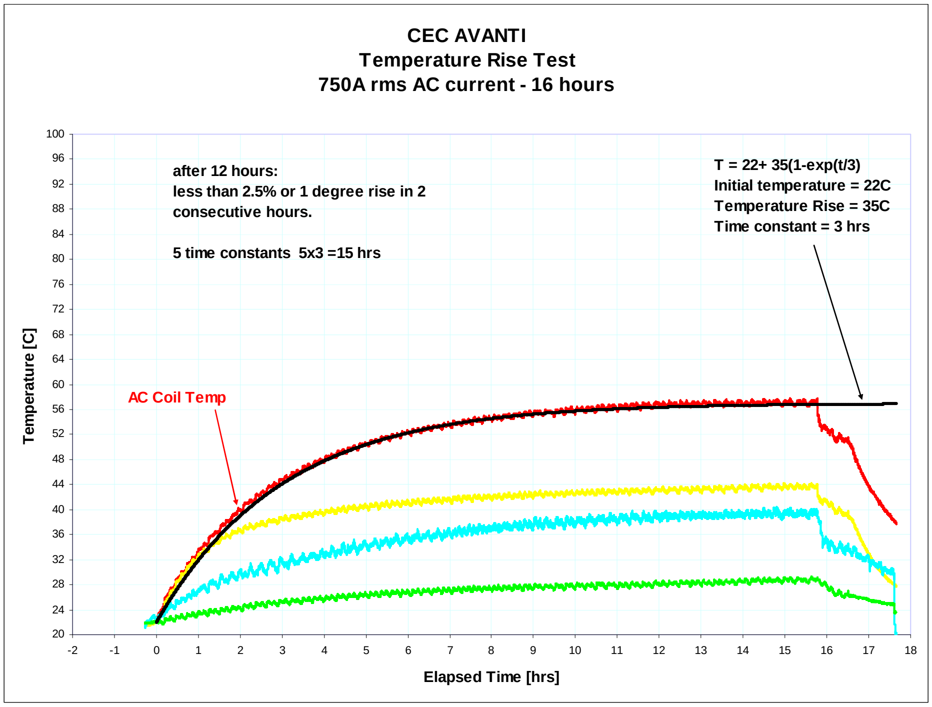


Figure 2: Measured temperatures during test phase

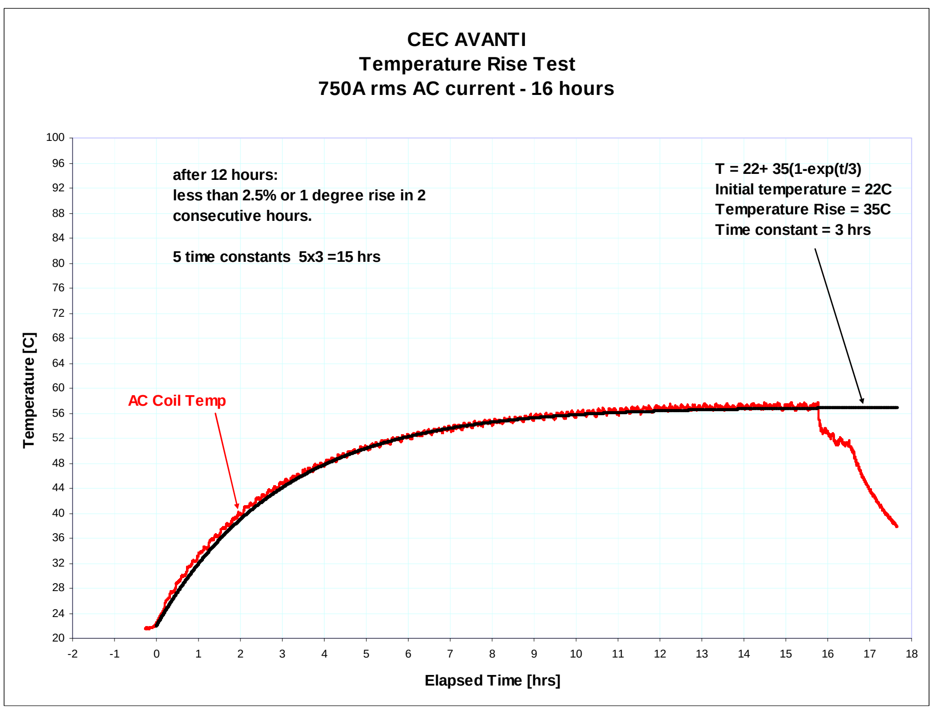


Figure 3: Measured temperature on AC coil during test

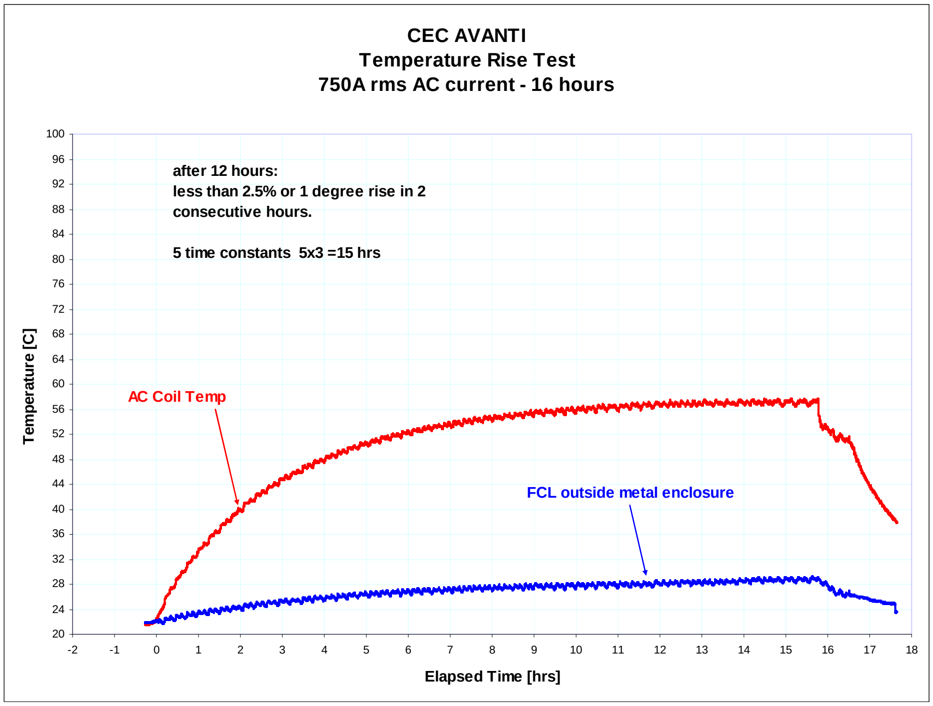


Figure 4: Measured results showing temperature level at metal enclosure

6. Thermo-graphic analysis

Figures 5-14 portray a thermo-graphic collection of images showing different parts of the FCL during the temperature rise test. This is very useful information since it allows understanding how heat is dissipated in the different elements of the FCL and their temperature range. It can also help to pinpoint unexpected hot spots on any of the elements or interconnection points.

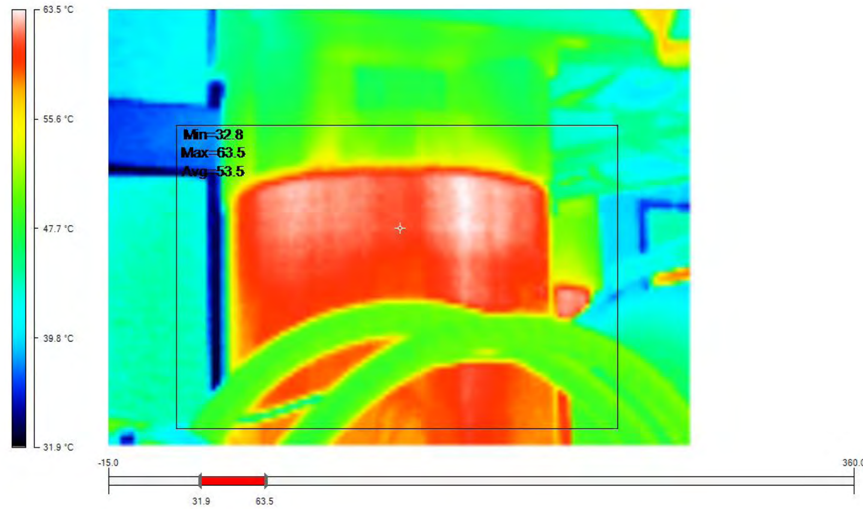


Figure 5: Temperature on top part of AC coil

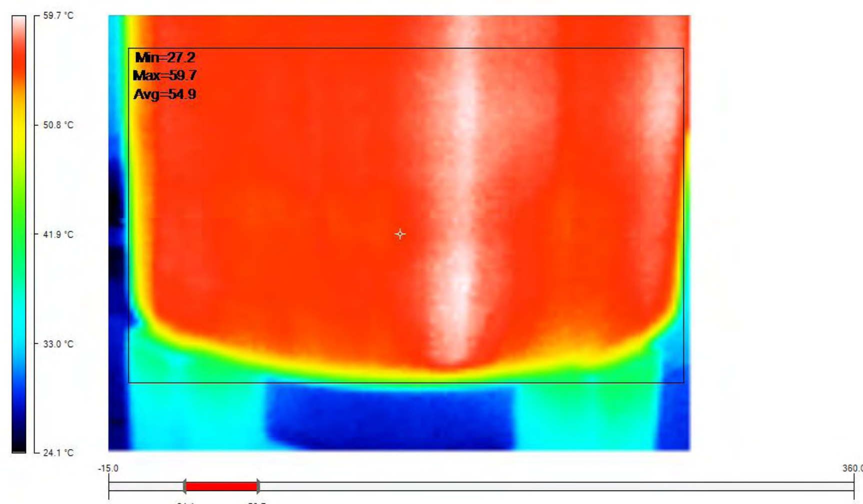


Figure 6: Temperature on bottom part of AC coil

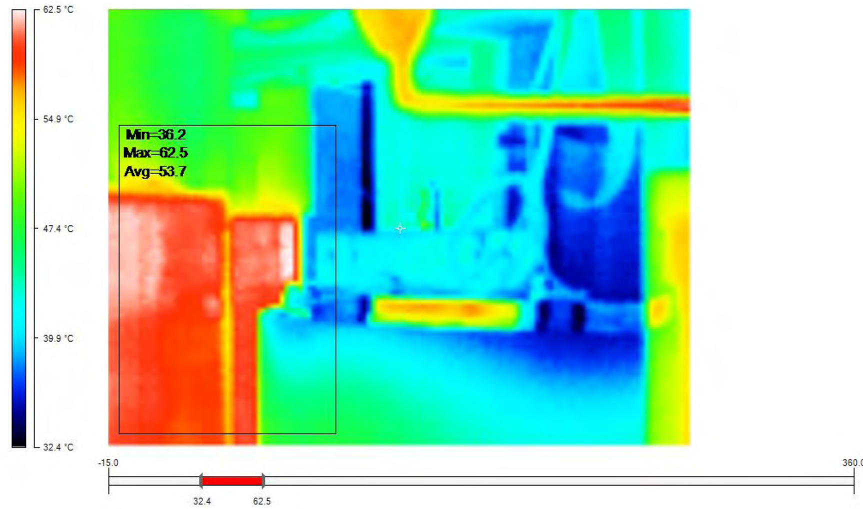


Figure7: View of AC coil and power cable with temperatures

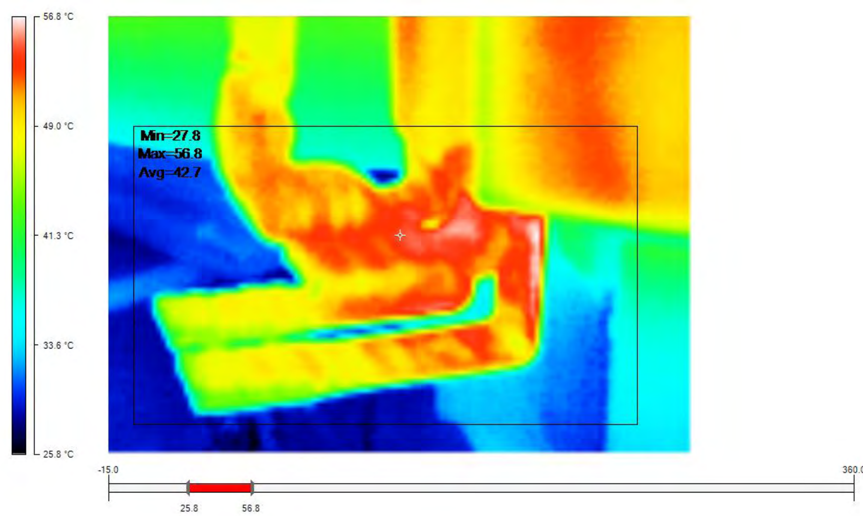


Figure 8: Temperature on AC coil termination

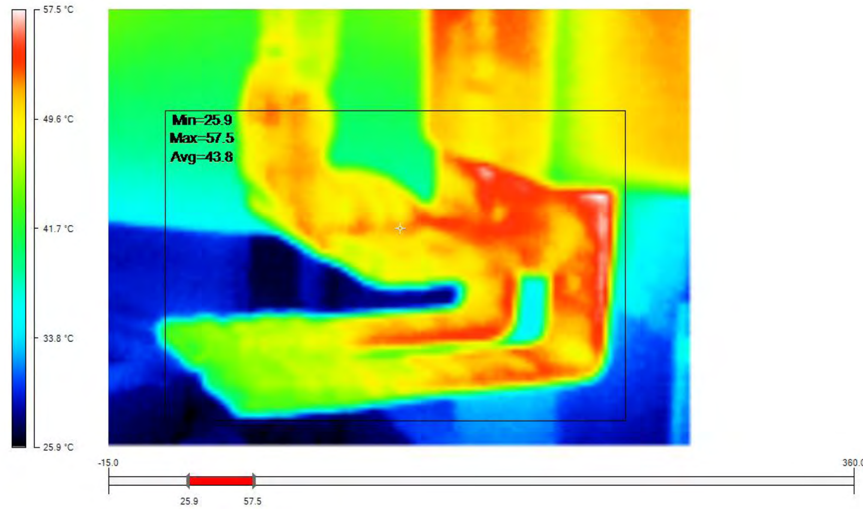


Figure 9: View of another AC coil termination

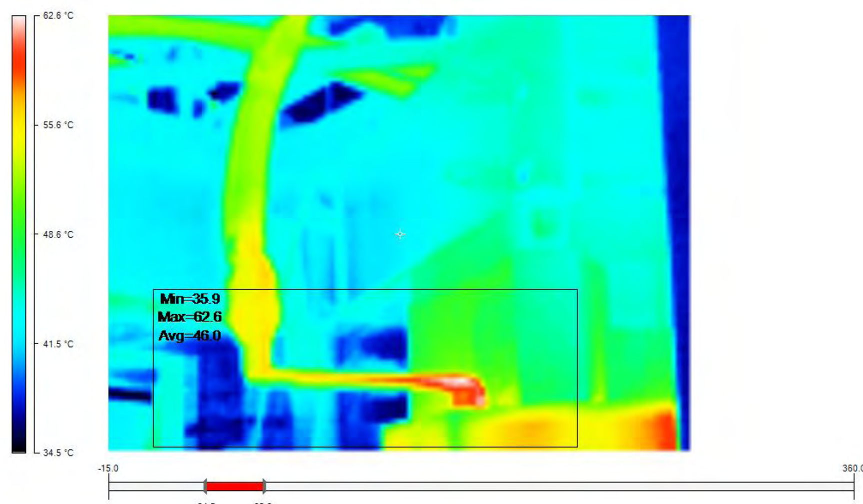


Figure10: Temperature on power cable jumper

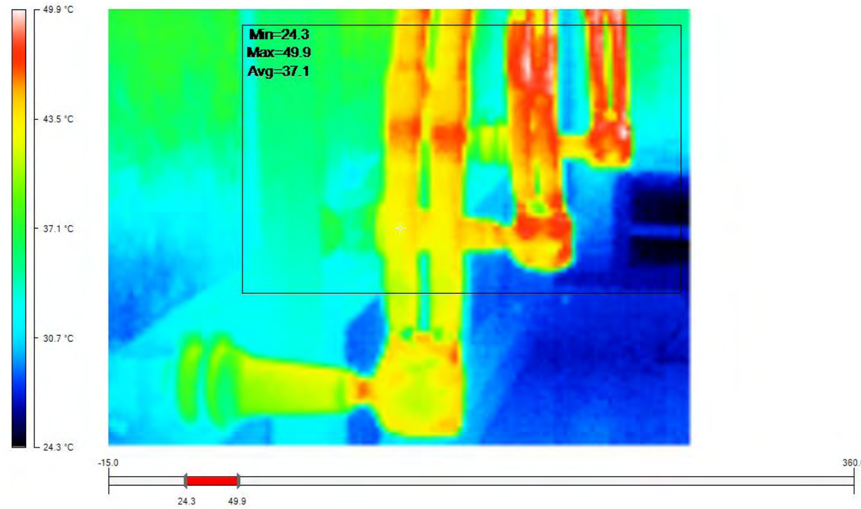


Figure 11: Temperature on cable jumpers from source side bushings to AC coils

Figure 12: A closer view to the bushing on the source side

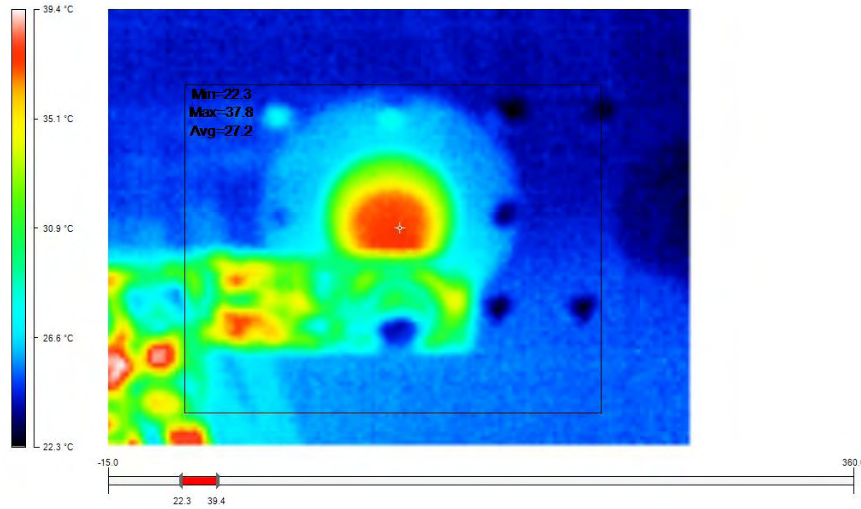


Figure13: View to a bushing on the outside of the FCL

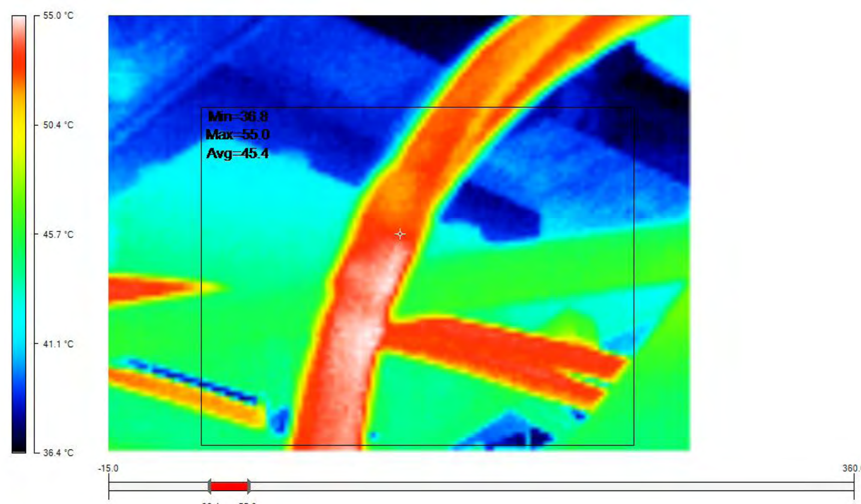


Figure14: Temperature on connecting cable jumper

7. Miscellaneous Photos

Figures 15 through 26 show different aspects and views of the FCL during the temperature rise test conducted at the Zenergy Power warehouse. Figure 15 is a view of the FCL with the power cables and bushings on the source side.

Figures 16 -19 depict several views on the 400 kW load banks with control boards displaying relevant parameters during test, while figure

20 is a view of the generator display showing L-N and L-L voltage, PF, current, frequency and kW.

Figure 21 is a closer view of the FCL on the source side. Figures 22-23 depict the monitored temperature during the test and figures 24-25 show the temperature on one of the bushings on the load side towards the end of the test.

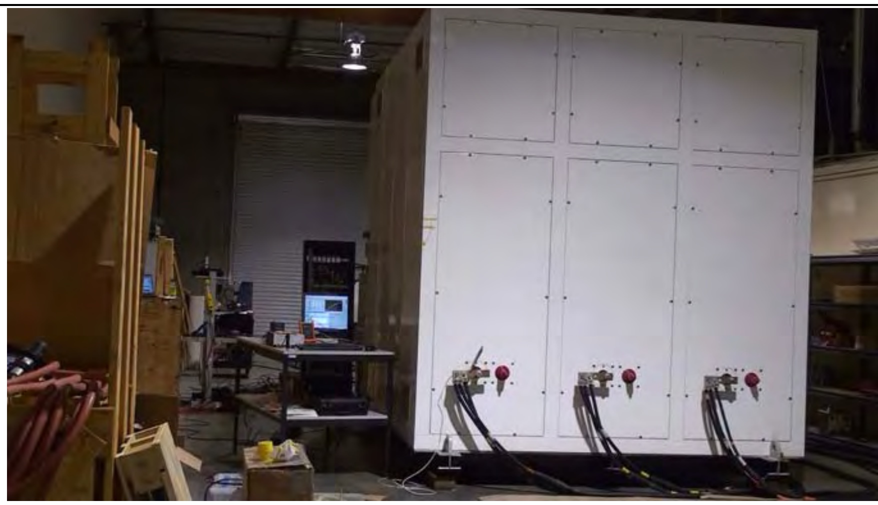


Figure 15: FCL view from the source side

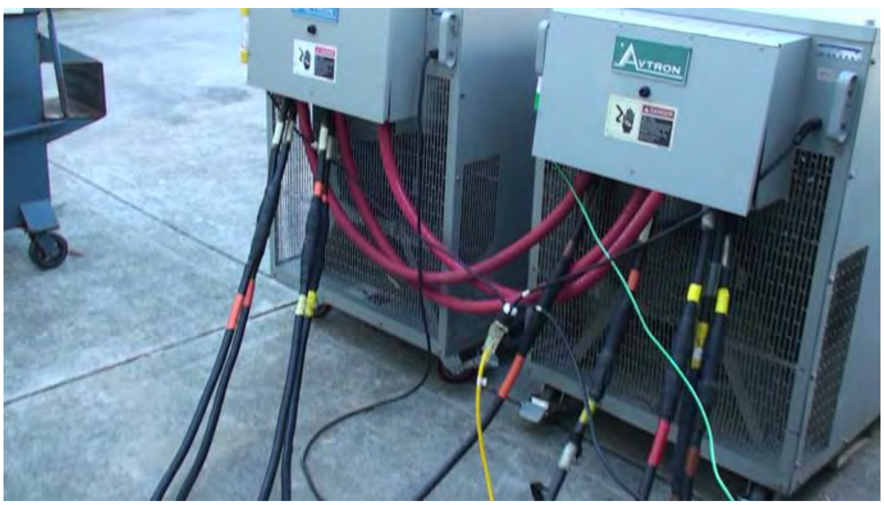


Figure 16: 400 kW load banks

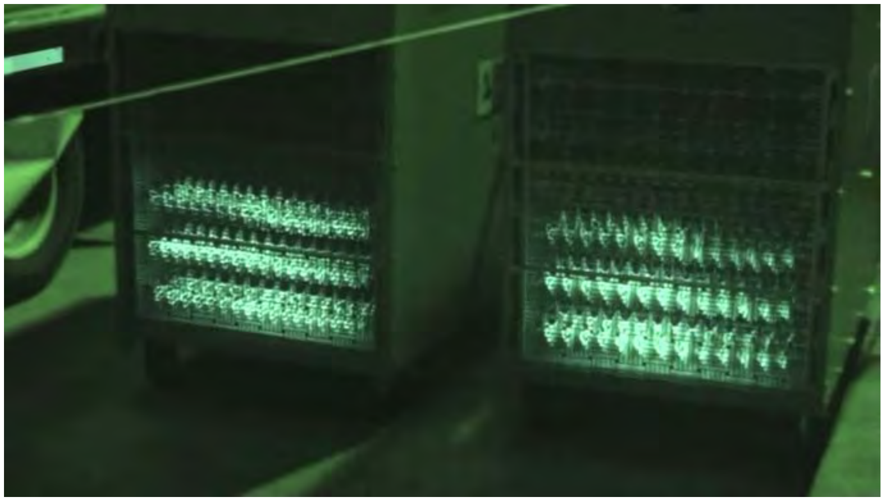


Figure 17: Load banks during temperature rise test

Figure 18: Control board on Load Bank 1 displaying current on the three phases

Figure 19: Control board on Load Bank 2 displaying phase-phase voltage, line current and kW power

Figure 20: Generator display showing operation parameters during the FCL temperature rise test

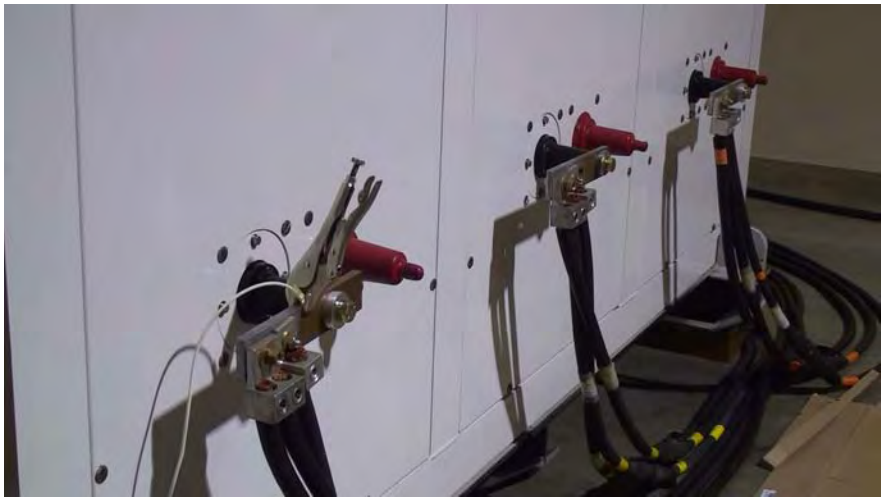


Figure 21: External view of the FCL on the source side

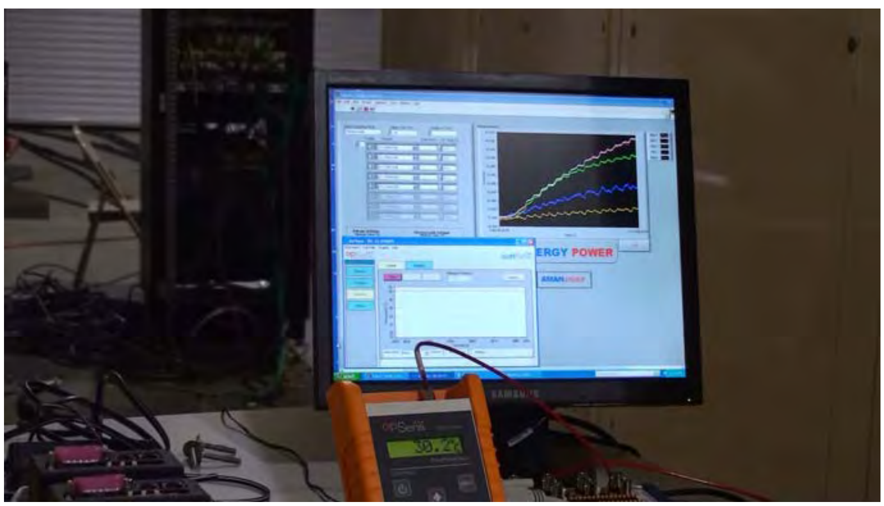


Figure 22: ZP monitor displaying measured temperatures during test

Figure 23: A closer view to figure 22

Figure 24: Thermo-graphic view of a bushing on the load side

Figure 25: Thermo-graphic view of a bushing on the load side as temperature falls at the end of the test

8. Conclusions

Results from the temperature rise test carried out on the Avanti FCL at Zenergy Power are presented in this report. The observed temperature rise on the AC coils was 35 degrees C above ambient temperature. The condition to reach this value per IEEE C57.12.01-1995 [4] was when temperature rise in the AC coils were less than 2.5% or 1% within two consecutive hours and the total time were at least 5 thermal constants. After 12 hours we had reached the first condition and the second condition was reached after 16 hours, taking into consideration that the measured thermal constant was equal to three hours.

We measured cryostat standby losses of 90 +/- 5 Watts, DC losses of 10 Watts approximately, and AC losses of 12 +/- 1 Watts. The induced AC losses in the HTS coil were measured at 95A DC and 751A AC.

9. List of Tables and Figures

List of Revisions

Revision	Date	Action	Modified Page
1	12/03/08	Released	

APPENDIX E:
Zenergy Power HTS FCL Short Circuit Test

Test Report

Reporting Center (full name and address):		Zenergy Power Inc. 379 Oyster Point Blvd., Suite 1 South San Francisco, CA USA 94080-1961 Tel.: +1-650-615-5700			
Responsible Person:	Franco Moriconi				
Project Name:	CEC Avanti				
Document Title:	**Fault Current Testing – Powertech High Power Labs 2008**				
Document Ref.No.:	**ZP/TR-2008/01**	Reg: #		Page 1	
Date of issue:	11/07/08	Classification:	Confidential	No. of pages:	97
Client(s):	CEC/SCE				
Author(s):	F. Moriconi F. De La Rosa A. Singh W. Schram	Approved:	F. Moriconi	Order No.:	
Distribution:	A. Kamiab, A. Hood (SCE), K. Smedley, L. Cibulka (CEC), C. Rose (LANL), F. Lambert (NEETRAC), B. Nelson, W. Gibson, A. Rodriguez, S. Ramsay (Zenergy USA), C. Buehrer, J. Keller (Zenergy DE), F. Darmann (Zenergy AUS)				
Distribution page 1:					
Keywords:	Fault Current Limiter, short circuit, prospective fault current, X/R ratio, fault level				

Summary:
The report presents the results of high-power short-circuit testing of Zenergy Power High-Temperature Superconducting Fault Current Limiter, performed from October 14 through October 17, 2008 at Powertech Labs in Surry, British Colombia Canada.

A total of 77 power and current tests were performed, including fault current calibration, voltage drop, full-power load, and fault current limiting tests. The Zenergy HTS FCL was energized at a nominal 12.47 kV three-phase line-to-line voltage, with a nominal steady-state current of up to 1,200 A.

The insertion impedance of the Zenergy HTS FCL (the steady-state voltage drop of the device when inserted into an electrical circuit) was measured repeatedly and found to be significantly less than 1% (on the order of .7% to .8%) at the nominal operating conditions expected for the Avanti Circuit.

Twenty-four fault current limiting tests were performed, including a series of tests with a maximum symmetrical fault current of 23 kA RMS and a first peak current of 63 kA. At the maximum prospective fault current of 23 kA, the Zenergy HTS FCL reduced the fault current by 19%. For the single-fault tests, the Zenergy HTS FCL was energized at the steady-state current and voltage levels, faulted for 30 cycles (one-half second), and returned to the steady-state conditions.

In addition to the standard single-fault tests, the Zenergy HTS FCL was subjected twice to a double-fault sequence of 20-cycle duration within a two-second time interval. The FCL performed extremely well under these conditions, successfully limiting both faults with no degradation in performance. The FCL was also subjected to an “endurance test” of a symmetrical 20 kA RMS fault current (with a 45 kA peak current) for more than 1.25 seconds. The Zenergy HTS FCL successfully clipped the protracted fault with no degradation.

Contents **Page**

1. Applicability

CEC Avanti HTS Fault Current Limiter 15kV class, 1200A

2. Applicable documentation

[1] Engineering Specification, ZP-ES-08-05 rev02 Test Protocol for FCL 15kV 1.2kA 3 Phase Use, ZP Internal Report.
[2] Engineering Report, ZP_ER-2008-02 - FCL Insertion Impedance Analysis.
[3] EEE Std C57.16-1996; IEEE Standard Requirements, Terminology, and Test Code for Dry-Type Air-core Series-Connected Reactors.
[4] CEC Avanti Test Plan 2 for the Avanti Fault Current Limiter at PowerTech

3. Acronyms and definitions

3.1 Acronyms

FCL	Fault Current Limiter
HTS	High Temperature Superconductor
CEC	California Energy Commission
SCE	Southern California Edison
POW	Point-On-Wave

3.2 Definitions

Xs	Source impedance - reactive
Rs	Source impedance - resistive
RL	Resistive load
TFR	Transformer
AUX	Auxiliary (circuit breaker for bolted 3-phase short circuit)
X/R	Reactive over resistive impedance ratio
Ia, Ib, Ic	Nominal current RMS, phase a, b and c
I_ss	Steady state current RMS
I_sc	Fault current - RMS
I_peak	Peak fault current
VD	Voltage Drop
L-L	Line to Line
L-G	Line to Ground

4. General

The report presents the results obtained during short circuit testing of Zenergy HTS FCL performed from October 14 through October 17, 2008 at Powertech High Power Lab test facility in Surry, British Colombia Canada.
Zenergy HTS FCL is a three-phase device designed to operate at 12.47 kV L-L voltage and 1,200 A steady-state current. The FCL is capable of clipping up to 23kA prospective fault current by 20% for multiple, rapidly reoccurring faults of up to 30 cycles (1/2 second) in duration. Under normal steady-state operating conditions the FCL

does not introduce harmonics and has extremely low insertion impedance; the voltage drop is less than 1% of the L-G bus voltage.

Section 6.1 of this report presents the results of the insertion impedance test. Section 6.2 presents the results of short circuit tests with the FCL in circuit, for prospective fault current RMS levels of 3, 8, 12.5, 15, 20 and 23kA.

5. Test Setup

The test circuit is illustrated below in Figure 1. Reactive and resistive source impedance components available at Powertech are given in Appendix D. The appropriate resistive and inductive loads were connected in delta configuration to generate the required steady state load current with a power factor of 0.9 approximately. The list of available resistive components is also given in Appendix D. A list of all short circuit and calibration tests is given in Table 1.

In the fault sequence, a make switch was first closed to supply load current for approximately 20 cycles. At the zero crossing of the voltage phase A the auxiliary switch was closed to apply a three phase to ground fault for a duration of 30 cycles. After the fault, the auxiliary switch was opened returning the circuit to normal load current for an additional 20 cycles. The sequence terminated with the final opening of the make switch.

The FCL was switched in and out of the circuit via the bypass breaker. To avoid the insertion of unaccountable impedances in the circuit, particular attention was devoted to calibrating the fault characterization with the bypass switch. Table 1 summarizes all the tests performed on the FCL.

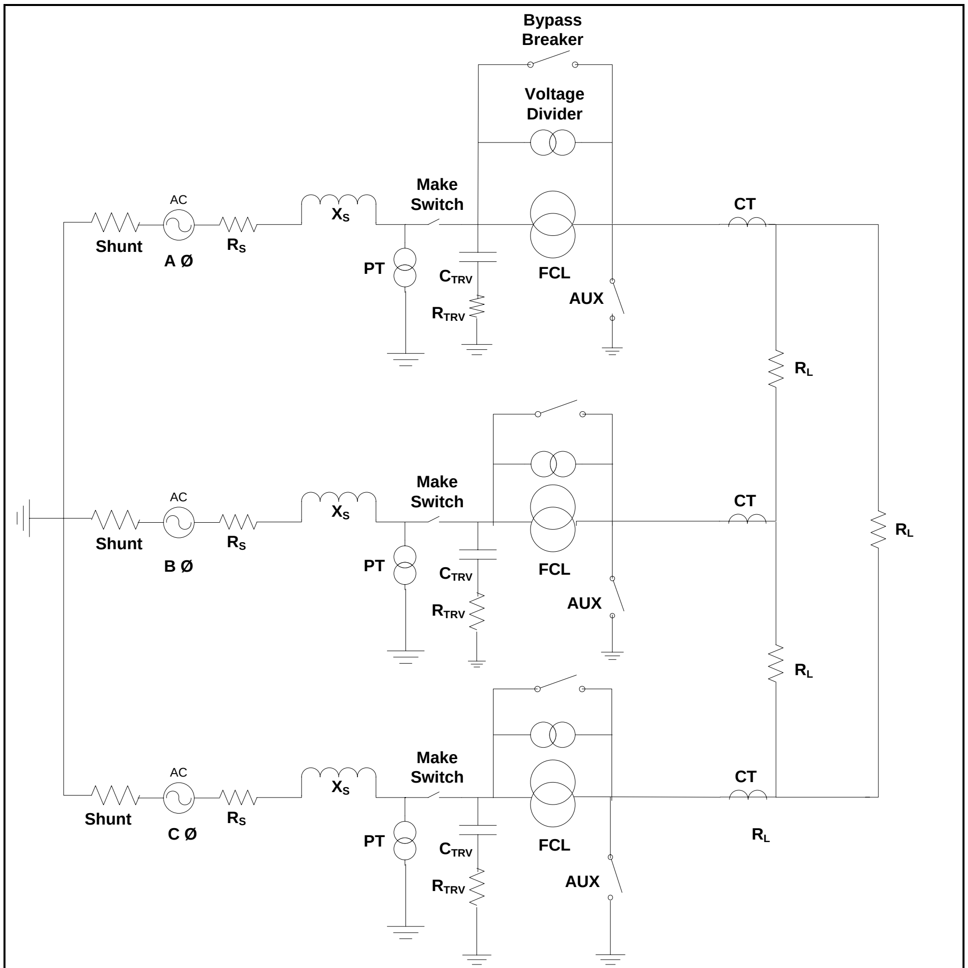


Figure 1: High power test circuit - Powertech Lab, Surry BC

Test ID	Date	Source Voltage kV	Type of test	FCL Status	Load Setting A	Load Actual A	Fault Level Setting kA	Fault Level Actual kA	X/R Ratio	DC Bias A	Notes
1	14-Oct	3.76	CAL	DISC			3		21.8	0	elbow-to-elbow connection
2	14-Oct	3.76	CAL	DISC			3	2.99	21.8	0	elbow-to-elbow connection
3	14-Oct	3.76	CAL	DISC	800	833			21.8	0	elbow-to-elbow connection
5	14-Oct	3.76	CAL	DISC	800	760				0	elbow-to-elbow connection
6	14-Oct	3.76	CAL	DISC	800	830			21.8	0	elbow-to-elbow connection
7	14-Oct	3.76	10-30-20	DISC	830	830	2.99	2.99	21.8	0	Head is too short
8	14-Oct	3.76	20-30-20	DISC	830	830	2.99	2.99	21.8	0	Not pure ASYM, RETAKE
9	14-Oct	3.76	20-30-20	DISC	830	830	2.99	2.99	21.8	0	GOOD. May have to adjust line current calibration in PT data
10	15-Oct	3.76	20-30-20	DISC	830	830	2.99	2.99	21.8	0	Calibration ob bypass switch. FCL disconnected and elbow are open. Adjuct line current calib for PT data.
11	15-Oct	3.76	20-30-20	BYPSD	830	830	2.99	2.99	21.8	0	Adjuct (1/2) line current calib for PT data.
12	15-Oct	3.76	CAL	BYPSD	830	830				100	GOOD
13	15-Oct	3.76	Load only	IN	830	830				100	GOOD
14	15-Oct	3.76	20-30-20	IN	830	830	2.99	2.99	21.8	100	GOOD. Adjust diff PT's scale factor
15	15-Oct	3.76	20-30-20	IN	830	830	2.99	2.99	21.8	100	File not aquired
16	15-Oct	3.76	20-30-20	IN	830	830	2.99	2.99	21.8	100	GOOD
17	15-Oct	3.76	20-30-20	IN	830	830	2.99	2.99	21.8	100	Retake of 15
18	15-Oct	3.76	20-30-20	IN	830	830	2.99	2.99	21.8	100	Retake of 16
19	15-Oct	3.76	CAL	BYPSD			5	5.1	24.8	100	
20	15-Oct	3.76	CAL	BYPSD	800	806				100	
21	15-Oct	3.76	20-30-20	IN	806	806	5.1	5.1	24.8	100	GOOD
22	15-Oct	3.76	20-30-20	BYPSD	806	806	5.1	5.1	24.8	100	GOOD, chech againt test 20
23	15-Oct	3.76	CAL	BYPSD			8	Low		100	Too low, retake
24	15-Oct	3.76	CAL	BYPSD			8	8.08	21.2	100	
25	15-Oct	3.76	CAL	BYPSD	800	821				100	
26	15-Oct	3.76	20-30-20	BYPSD	821	821	8.08	8.08	21.2	100	GOOD
27	15-Oct	3.76	20-30-20	IN	821	821	8.08	8.08	21.2	100	GOOD
28	15-Oct	3.76	CAL	BYPSD			10	Low		100	
29	15-Oct	3.76	CAL	BYPSD			10	10.2	21.2	100	
30	15-Oct	3.76	CAL	BYPSD	800	824				100	
31	15-Oct	3.76	20-30-20	BYPSD	824	824	10.2	10.2	21.2	100	GOOD
32	15-Oct	3.76	20-30-20	IN	824	824	10.2	10.2	21.2	100	GOOD
34	15-Oct	3.76	CAL	BYPSD			12.5	12.5	21.1	100	
35	15-Oct	3.76	CAL	BYPSD	800	825				100	
36	15-Oct	3.76	20-30-20	BYPSD	825	825	12.5	12.5	21.1	100	GOOD
37	15-Oct	3.76	20-30-20	IN	825	825	12.5	12.5	21.1	100	GOOD, Flashover
38	15-Oct	3.76	20-20-20	IN	825	825	12.5	12.5	21.1	100	Reduced num of fault cycles
39	15-Oct	3.76	20-30-20	IN	825	825	12.5	12.5	21.1	100	GOOD
40	16-Oct	3.76	20-30-20	IN	825	825	12.5	12.5	21.1	140	GOOD
41	16-Oct	13.1	CAL	BYPSD	300	330				100	
42	16-Oct	13.1	CAL	BYPSD	330	330				100	Differential PT's high noise Phase C
43	16-Oct	13.1	CAL	BYPSD	330	330				100	
44	16-Oct	13.1	Load only	IN	330	330				100	GOOD
45	16-Oct	13.1	CAL	BYPSD	500	520				100	
46	16-Oct	13.1	Load only	IN	520	520				100	GOOD
47	16-Oct	13.1	CAL	BYPSD	750	751				100	
48	16-Oct	13.1	Load only	IN	751	751				100	GOOD
49	16-Oct	13.1	CAL	BYPSD	1000	1001				100	
50	16-Oct	13.1	Load only	IN	1001	1001				100	GOOD
51	16-Oct	13.1	CAL	BYPSD	1200	1201				100	
52	16-Oct	13.1	Load only	IN	1201	1201				100	Differential PT's out of range, Retake
53	16-Oct	13.1	Load only	IN	1201	1201				100	GOOD
54	16-Oct	13.1	Load only	IN	1001	1001				142	GOOD
55	16-Oct	13.1	Load only	IN	1001	1001				160	GOOD
56	16-Oct	13.1	CAL	BYPSD	800		3		19	140	X/R too low, retake
57	16-Oct	13.1	CAL	BYPSD	820		3	3.02	22.9	140	
58	16-Oct	13.1	CAL	BYPSD	820					140	Missed data due to calibration
59	16-Oct	13.1	CAL	BYPSD	800	838				140	
60	16-Oct	13.1	20-30-20	BYPSD	838	838	3.02	3.02	22.9	140	GOOD
61	16-Oct	13.1	20-30-20	IN	838	838	3.02	3.02	22.9	140	GOOD
62	16-Oct	13.1	20-30-20	BYPSD	816	816	8	8.05	19.8	140	GOOD
63	16-Oct	13.1	20-30-20	IN	816	816	8.05	8.05	19.8	140	GOOD
64	16-Oct	13.1	20-30-20	BYPSD	800	787	12	12.42	19.7	140	GOOD
65	16-Oct	13.1	20-30-20	IN	787	787	12.42	12.42	19.7	140	GOOD
66	17-Oct	13.1	CAL	BYPSD	800	780	15		31.2	140	X/R too high, retake
67	17-Oct	13.1	CAL	BYPSD			15	15.2	26.3	140	
68	17-Oct	13.1	CAL	BYPSD			20		21	140	Our CT's overload, >45,450A
69	17-Oct	13.1	CAL	BYPSD			23	23	44	140	
70	17-Oct	13.1	20-30-20	IN	780	780	15.2	15.2	26.3	140	GOOD
71	17-Oct	13.1	20-30-20	IN	780	780	20	20	21.6	140	GOOD
72	17-Oct	13.1	20-30-20	IN	780	780	23	23	44	140	Flash Over
73	17-Oct	13.1	20-30-20	IN	780	780	23	23	44	140	Flash Over
74	17-Oct	13.1	CAL	IN	300						Changed bus-bar supports. Low amps for a few cycles
75	17-Oct	13.1	20-30-20	IN	780	780	23	23	44	140	GOOD
76	17-Oct	13.1	Double Fault 0-20-120-20-30	IN	800	800	20	20	21	140	DAQ out of memeory, must RETAKE
77	17-Oct	13.1	Double Fault 0-20-120-20-30	IN	800	800	20	20	21	140	Error in timing. Single fault up to 1.25 sec = 80 Cycles
78	17-Oct	13.1	Double Fault 0-20-120-20-30	IN	800	800	20	20	21	140	GOOD

Table 1: List of short circuit tests

6. Results

6.1 FCL Insertion Impedance

The test circuit was configured with a 60 Hz, 13.1 kV L-L source. Source and load impedances were adjusted to ensure a bus voltage of 12.4kV and a power factor close to 0.9. Baseline measurements were performed at load currents of 330, 520, 750, 1000, and 1200 A. The voltage drop across each phase was measured with differential PT's.

Table 2 below shows the insertion impedance results in terms of maximum voltage drop across each phase. The voltage drop is also computed as a percentage of 12.4kV L-L voltage. The DC bias current in the HTS coil was kept constant at 100A. Two tests at 1000A ac load were repeated with the DC bias increased from 100 to 140A, and to 160A.

Figures 2-4 show the FCL voltage drop as a function of AC load and DC bias.

The FCL insertion impedance was well predicted and accurately measured. The FCL voltage drop was found to be below 1% for all load currents expected at the Avanti circuit (max load current of 750A.) The FCL did not introduce any harmonics into the system.

Line current waveforms and plots of voltage drop can be found in APPENDIX A.

Test ID	Source Voltage kV	Load Actual A	DC Bias A	VD ph_A FCL in V	VD ph_B FCL in V	VD ph_C FCL in V	Average 3 phases V	Max 3 phases V	Voltage Drop percent of 12.47kV
44	13.1	**330**	100	20.4	18.8	21.8	20.3	**21.8**	**0.30%**
46	13.1	**520**	100	35.8	32.8	35.2	34.6	**35.8**	**0.50%**
48	13.1	**751**	100	64.3	58.6	62.4	61.8	**64.3**	**0.89%**
50	13.1	**1001**	100	135	123	132	130.0	**135.0**	**1.88%**
53	13.1	**1201**	100	222	206	217	215.0	**222.0**	**3.08%**
54	13.1	**1001**	142	118	107	115	113.3	**118.0**	**1.64%**
55	13.1	**1001**	160	109	100	107	105.3	**109.0**	**1.51%**

Table 2: Voltage Drop Results Summary

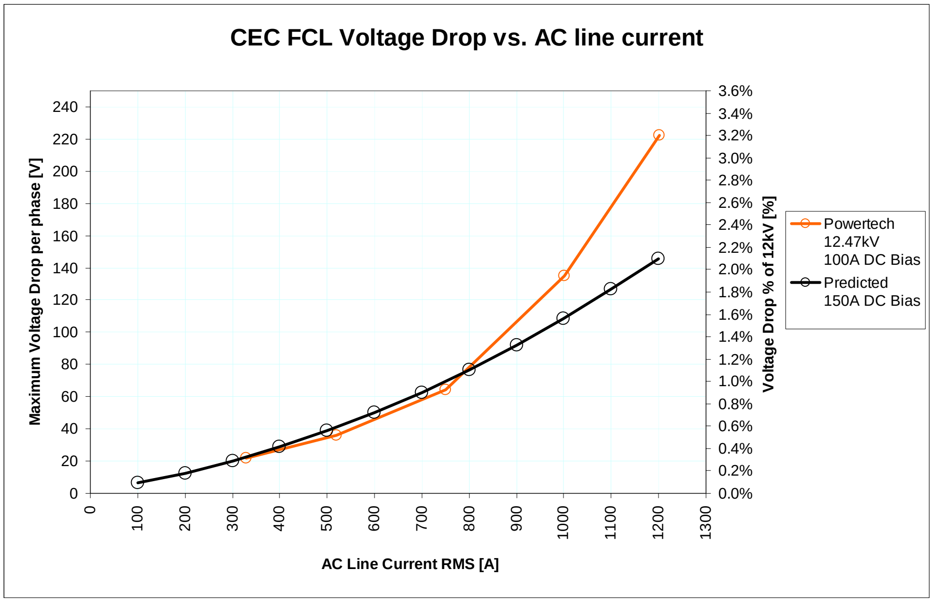


Figure 2: FCL Voltage Drop vs. AC line current

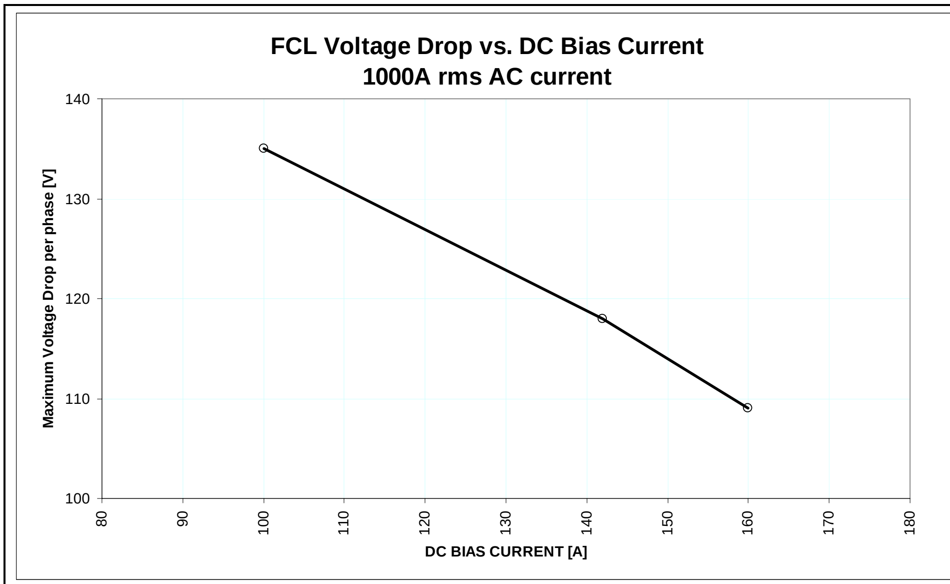


Figure 3: FCL Voltage Drop vs. DC Bias current

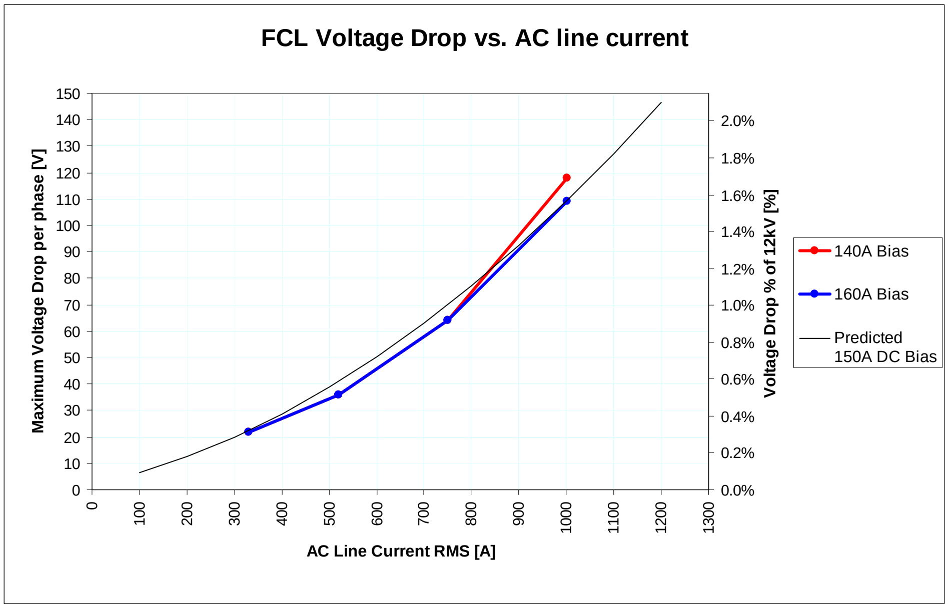


Figure 4: FCL Voltage Drop vs. AC current and DC Bias

6.2 FCL Fault Current Test results

The same test circuit with a power source of 13.1kV L-L was configured to provide 20 cycles of load current, followed by 30 cycles of fault current, followed by a fault clearance and return to load conditions for 20 cycles. Fault current characterization tests were performed with the FCL disconnected and/or bypassed in order to determine the appropriate source impedance values capable of generating prospective fault current RMS levels of : 3, 8, 12.5, 15, 20, 23 kA, with X/R ratios of more than 21. All faults were bolted 3 phase to ground.

Table 3 below shows the FCL clipping performance as a percentage of symmetric prospective fault current. The maximum fault reduction was measured to be 20% of a 20kA symmetric prospective fault.

Figure 5 shows the same results in a plot format. Note that for the 23kA fault level, the measured X/R ratio was 44, whereas the predicted clipping was computed for an X/R ratio of 21.

Table 5 shows the FCL clipping of the maximum peak fault. Peak clipping was measured at 15-16% for fault levels between 15kA and 23kA. Figure 7 shows the single phase fault current reduction for the 23kA fault level. All fault current reduction waveforms can be found in Appendix B.

Test ID	Fault Level Actual kA	X/R Ratio	DC Bias A	Fault I_A FCL in kA	Fault I_B FCL in kA	Fault I_C FCL in kA	Average 3 phases kA	Max 3 phases kA	Clipping Symmetric
61	3.02	22.9	140	2.78	2.75	2.76	2.8	2.8	7.9%
63	8.05	19.8	140	6.83	6.98	6.96	6.9	7.0	13.3%
65	12.42	19.7	140	10.2	10.4	10.4	10.3	10.4	16.3%
70	15.2	26.3	140	12.3	12.5	12.4	12.4	12.5	17.8%
71	20	21.6	140	15.7	16	15.7	15.8	16.0	20.0%
75	23	44	140	18	18.6	18.4	18.3	18.6	19.1%

Table 3: Fault Clipping Results Summary

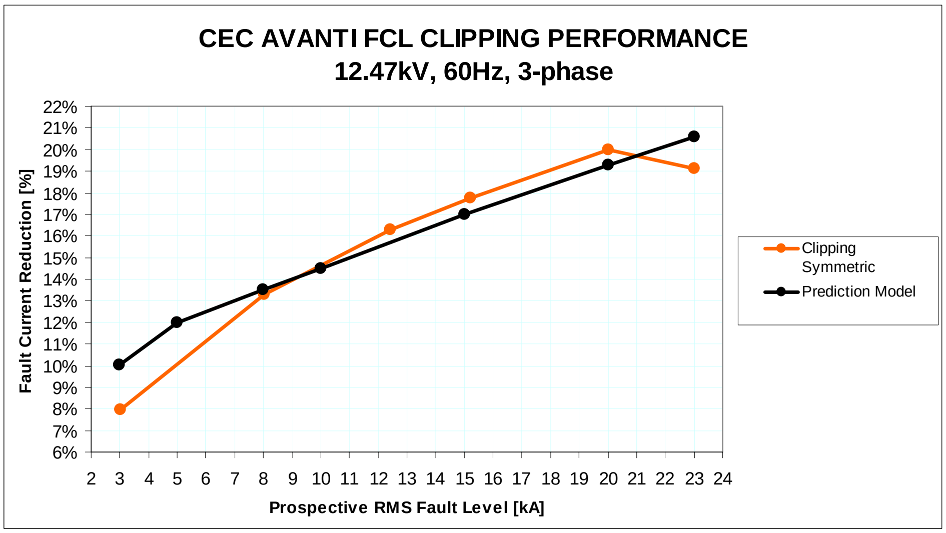


Figure 5: Percent Clipping vs. prospective fault level (Note: at 23kA X/R=44 vs. 21 in prediction model)

Test ID	Fault Level Actual kA	Peak Fault prospective kA	X/R Ratio	DC Bias A	Fault I_A Peak kA	Fault I_B Peak kA	Fault I_C Peak kA	Max clipped Peak kA	Peak Clipping
61	3.02	7.4	22.9	140	6.2	6.5	5.4	6.5	11.1%
63	8.05	20.8	19.8	140	18.7	17.7	10.9	18.7	10.2%
65	12.42	31.4	19.7	140	27.6	19.1	24.3	27.6	12.2%
70	15.2	40.3	26.3	140	20.9	34.2	30.9	34.2	15.1%
71	20	52.4	21.6	140	27.7	43.6	38.4	43.6	16.8%
75	23	63.1	44	140	28.1	53.2	48.6	53.2	15.7%

Table 4: Peak Fault Clipping Results Summary

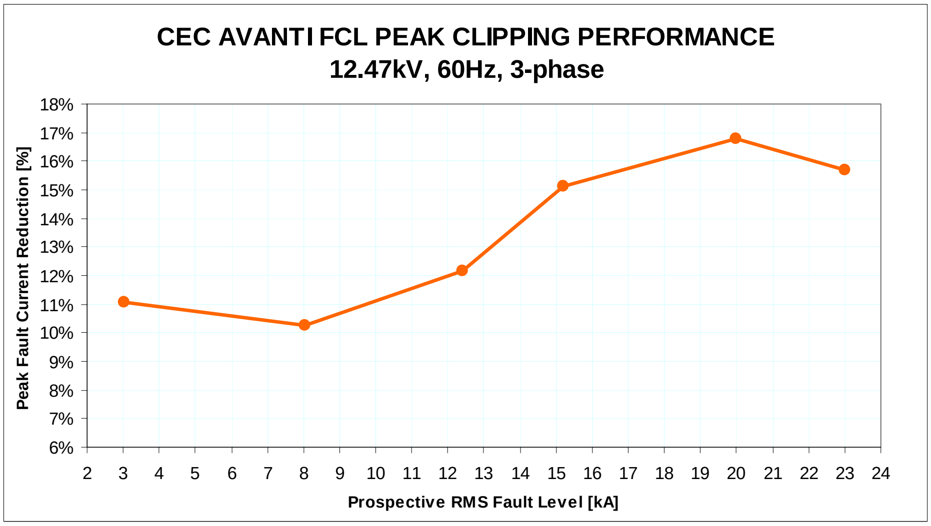


Figure 6: Percent Peak Clipping vs. prospective fault level

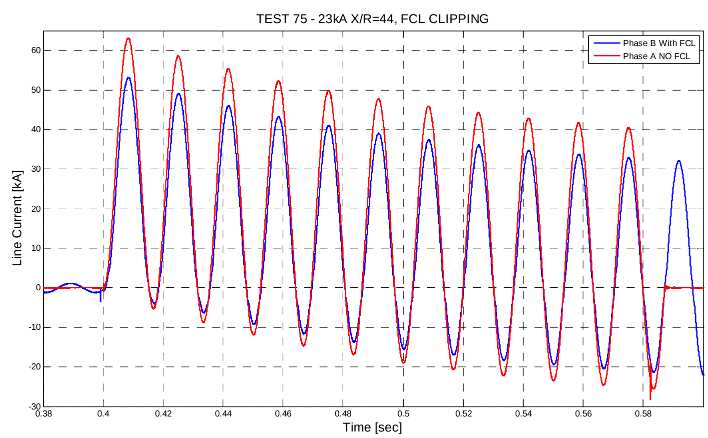


Figure 7: FCL Clipping of 23kA fault – single phase

7. List of Tables and Figures

8. APPENDIX A – Insertion impedance and Voltage drop

8.1 TEST 43 - 330 A RMS LOAD CURRENT - NO FCL

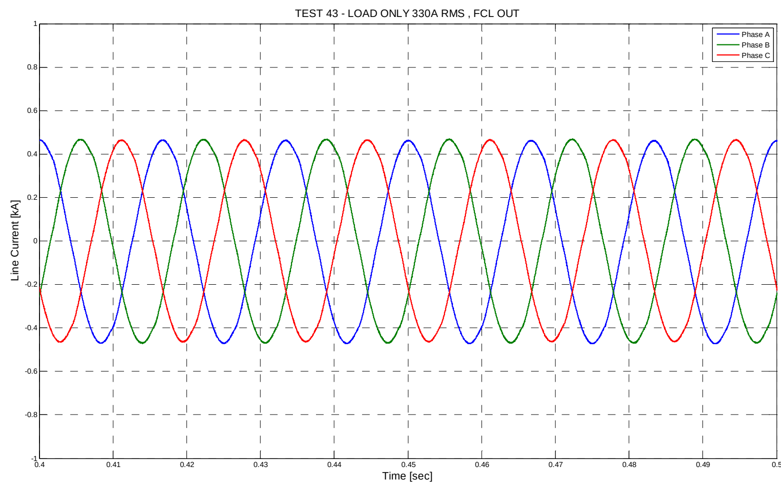


Figure A1: 330A RMS load current – FCL Bypassed

8.2 TEST 44 - 330 A RMS LOAD CURRENT with FCL

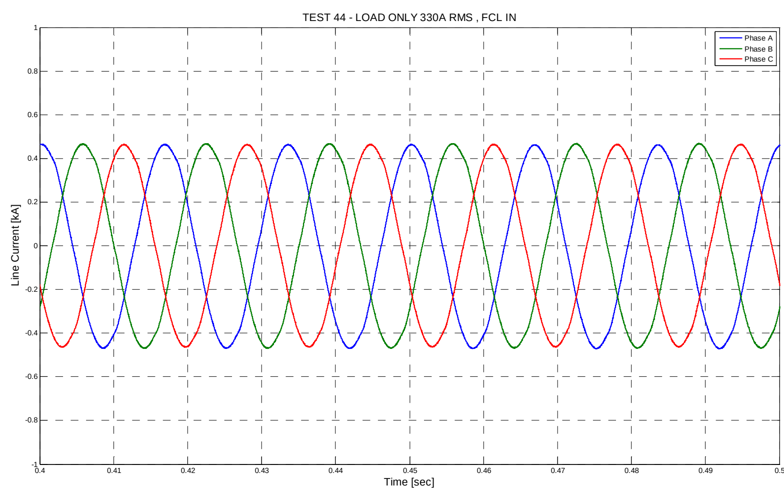


Figure A2: 330A RMS load current – FCL IN

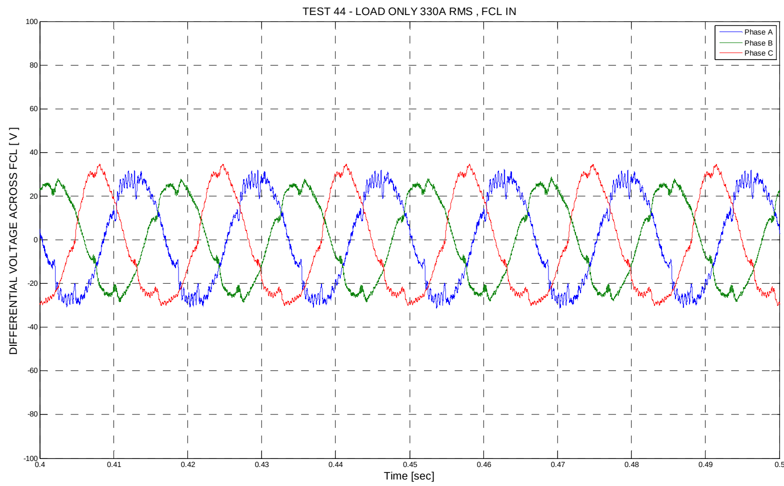


Figure A3: Voltage Drop at 330A load current

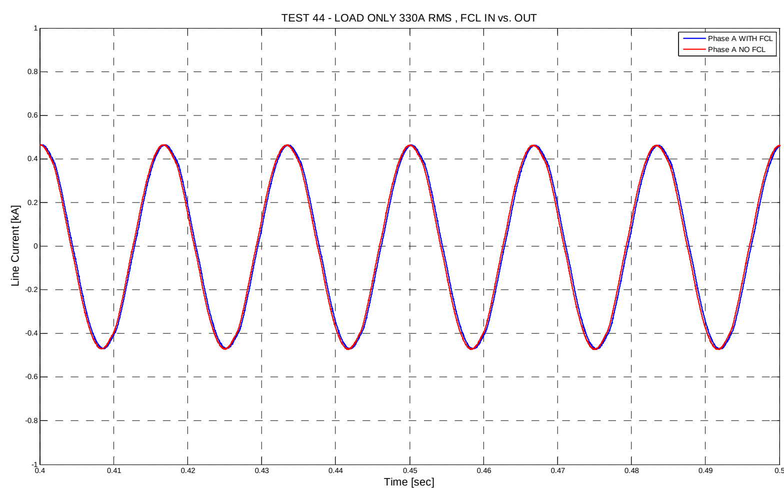


Figure A4: Line Current Ph A - 330A FCL IN vs. OUT

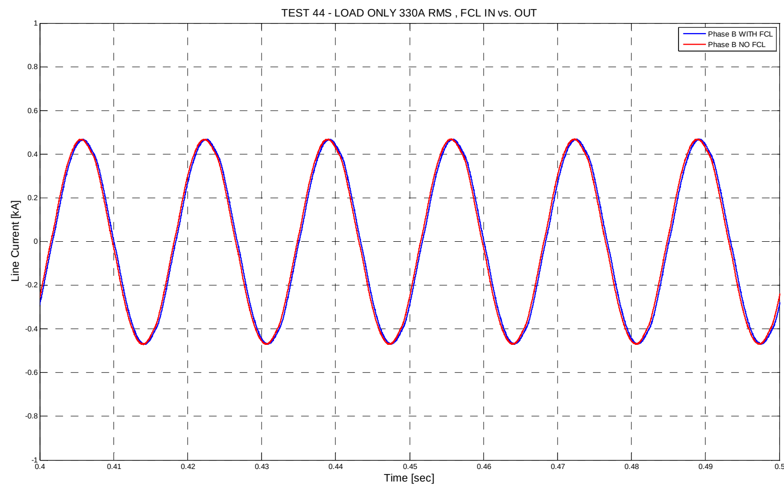


Figure A5: Line Current Ph B - 330A FCL IN vs. OUT

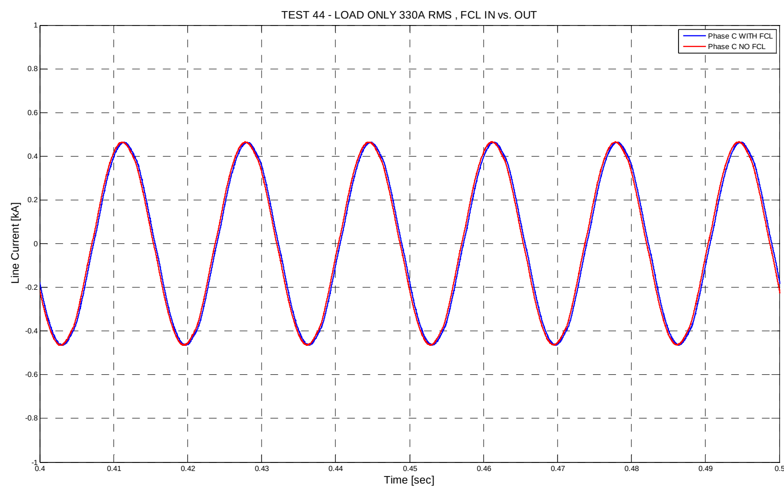


Figure A6: Line Current Ph C - 330A FCL IN vs. OUT

8.3 TEST 45 - 520 A RMS LOAD CURRENT NO FCL

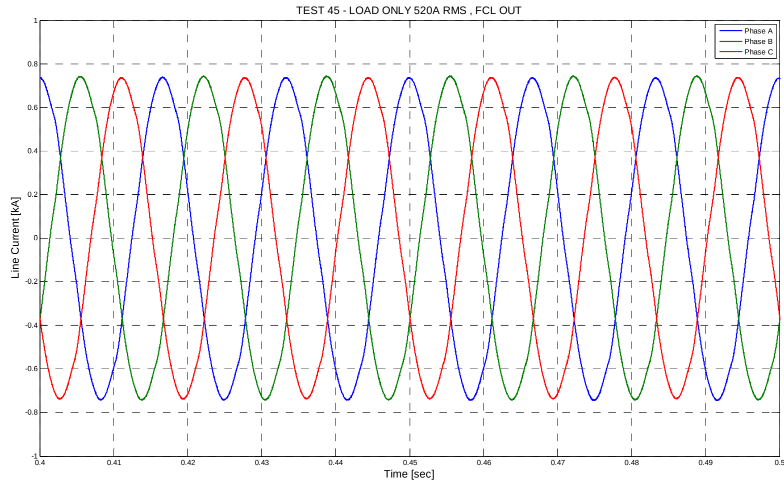


Figure A7: 520A RMS load current – FCL Bypassed

8.4 TEST 46 - 520 A RMS LOAD CURRENT

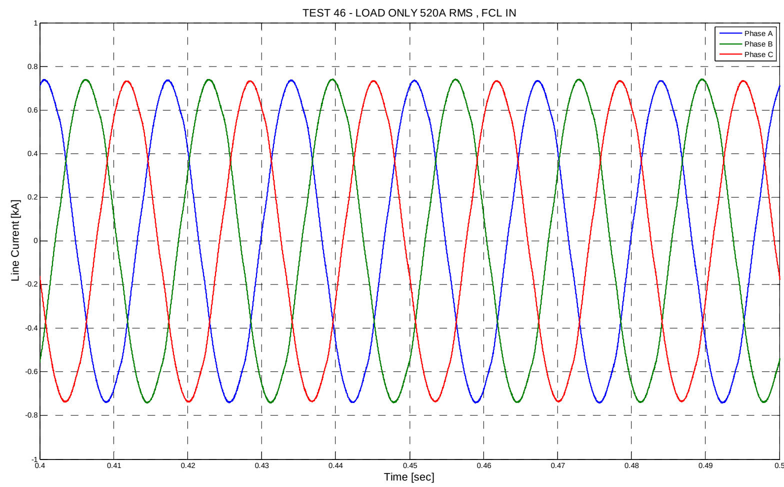


Figure A8: 520A RMS load current – FCL IN

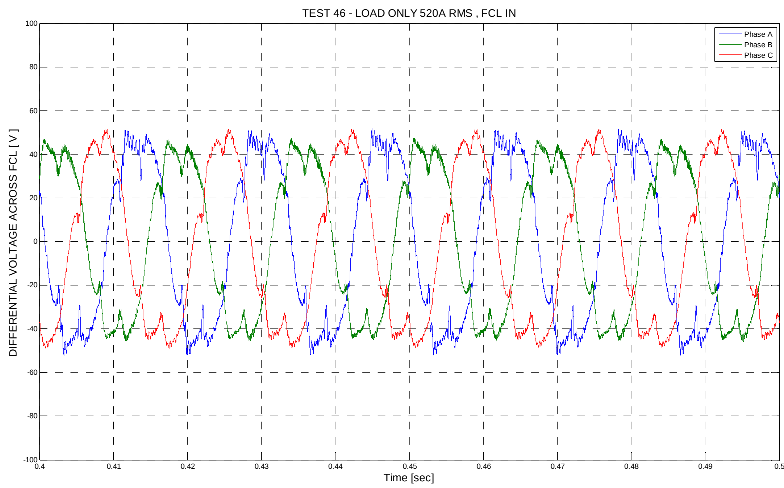


Figure A9: Voltage Drop at 520A load current

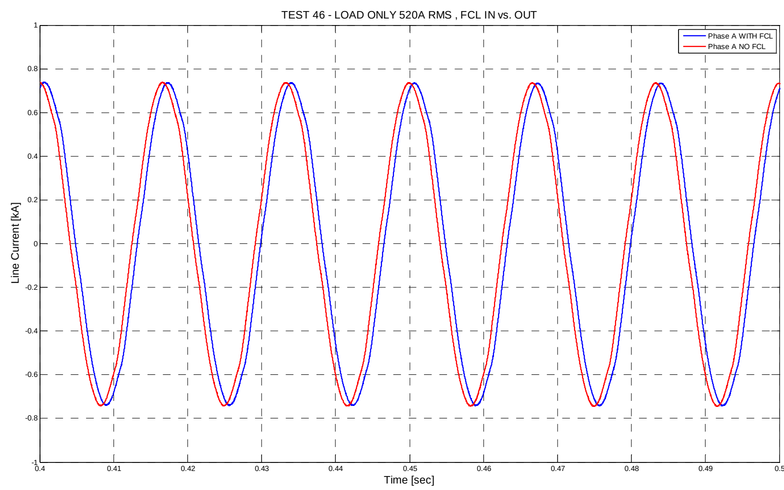


Figure A10: Line Current Ph A - 520A FCL IN vs. OUT

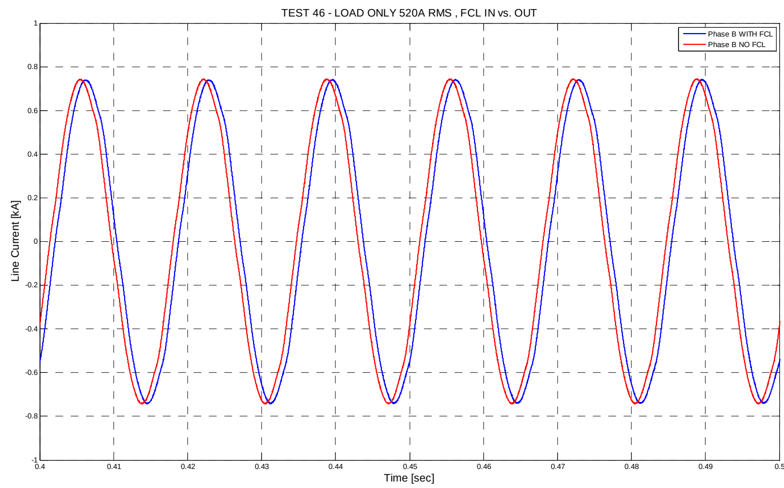


Figure A11: Line Current Ph B - 520A FCL IN vs. OUT

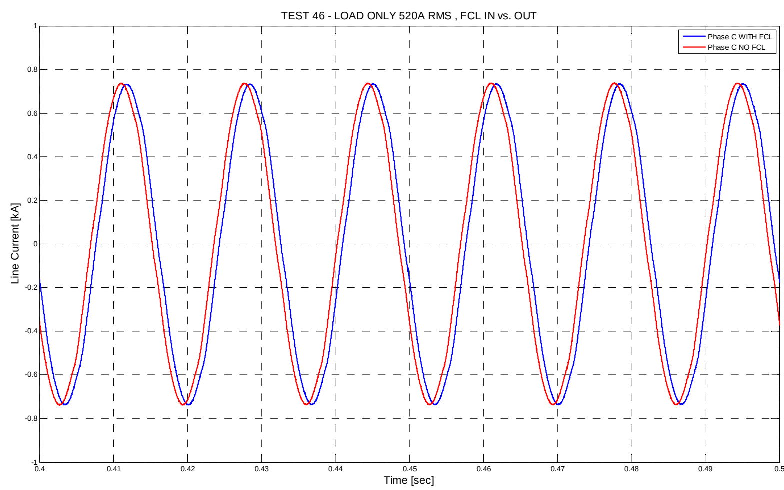


Figure A12: Line Current Ph C - 520A FCL IN vs. OUT

8.5 TEST 47 - 750 A RMS LOAD CURRENT NO FCL

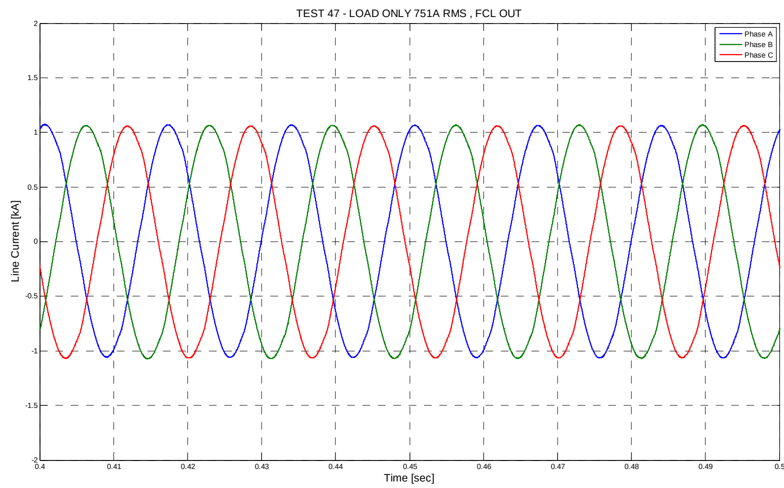


Figure A13: 750A RMS load current – FCL Bypassed

8.6 TEST 48 - 750 A RMS LOAD CURRENT

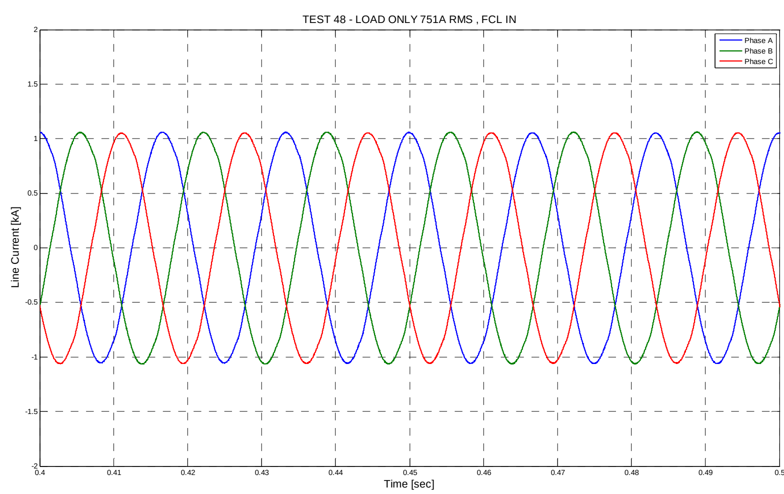


Figure A14: 750A RMS load current – FCL IN

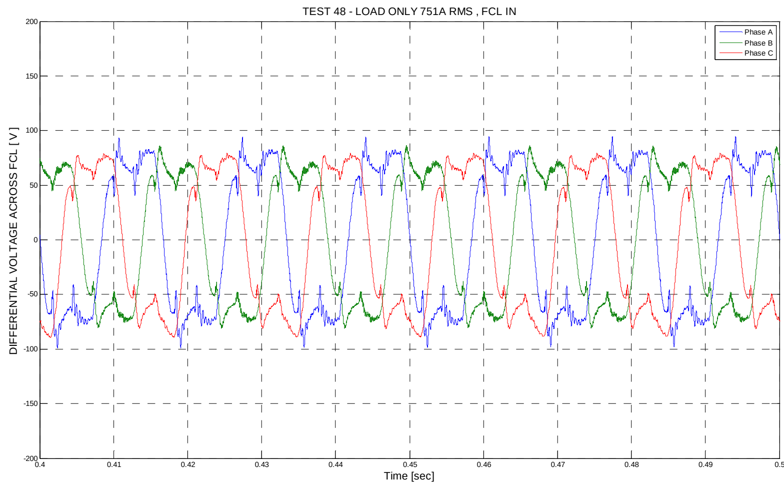


Figure A15: Voltage Drop at 750A load current

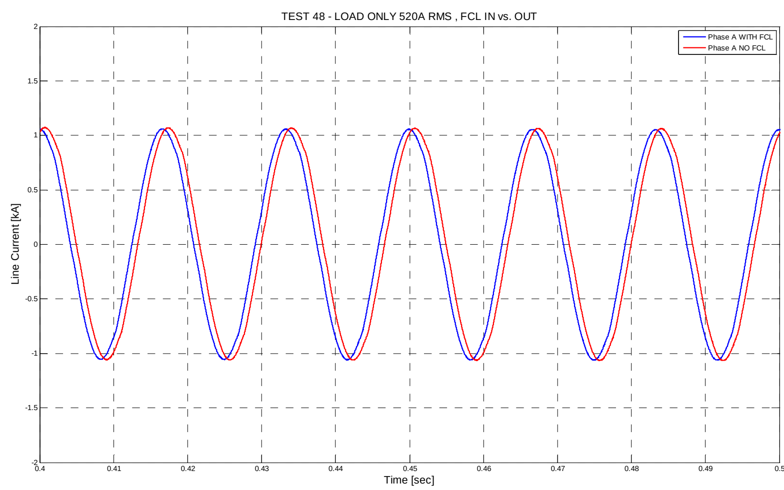


Figure A16: Line Current Ph A - 750A FCL IN vs. OUT

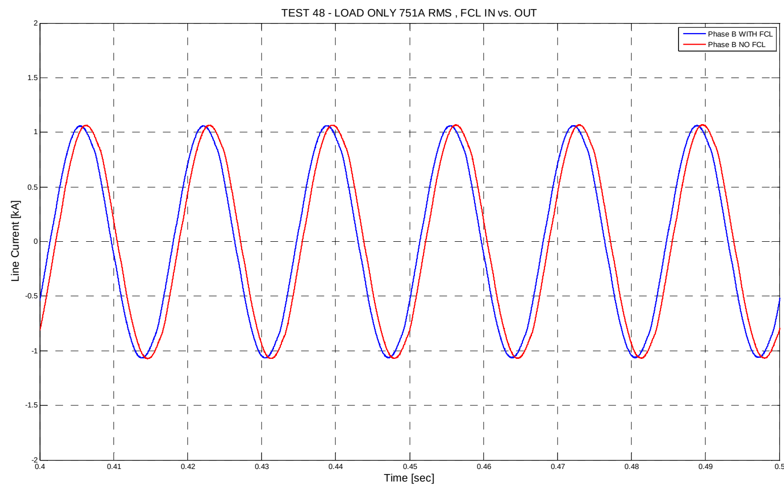


Figure A17: Line Current Ph B - 750A FCL IN vs. OUT

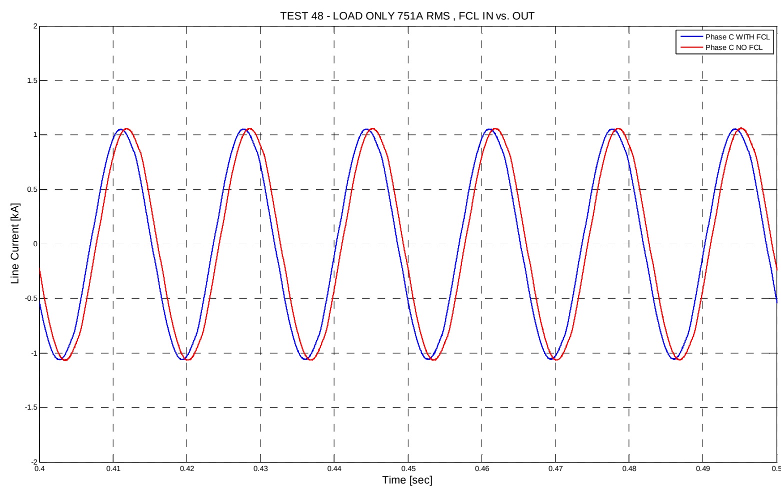


Figure A18: Line Current Ph C - 750A FCL IN vs. OUT

8.7 TEST 49 - 1000 A RMS LOAD CURRENT NO FCL

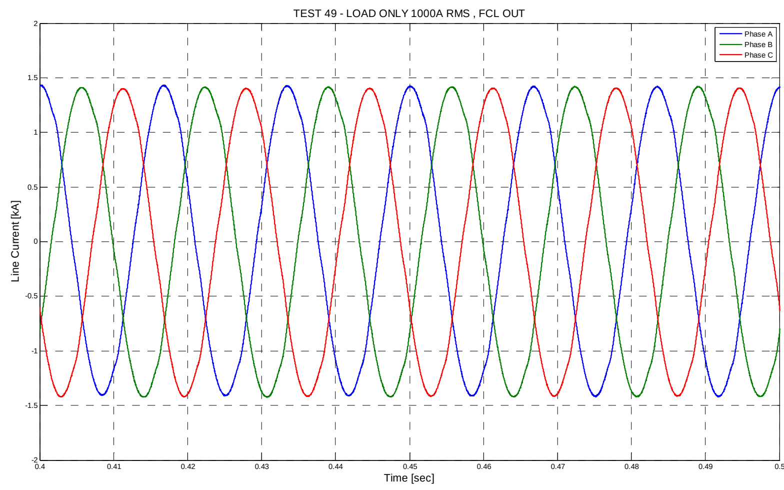


Figure A19: 1000A RMS load current – FCL Bypassed

8.8 TEST 50 - 1000 A RMS LOAD CURRENT

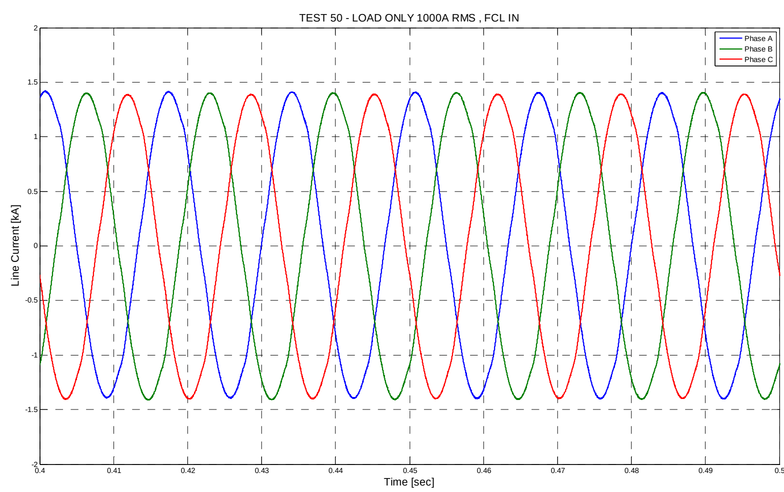


Figure A20: 1000A RMS load current – FCL IN

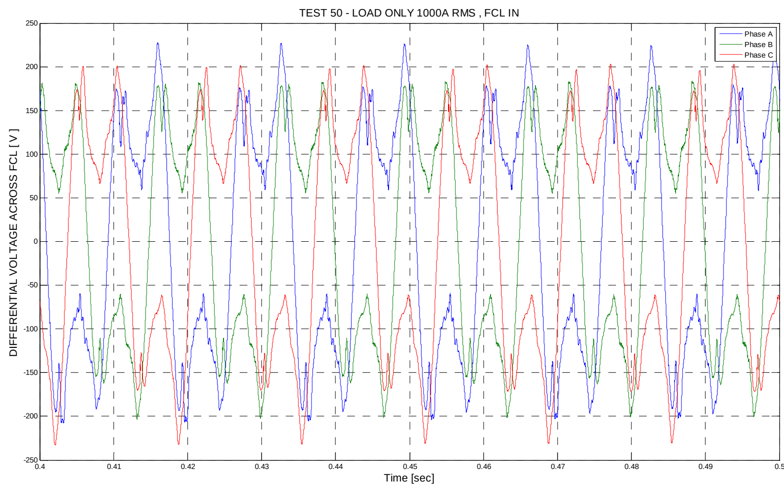


Figure A21: Voltage Drop at 1000A load current

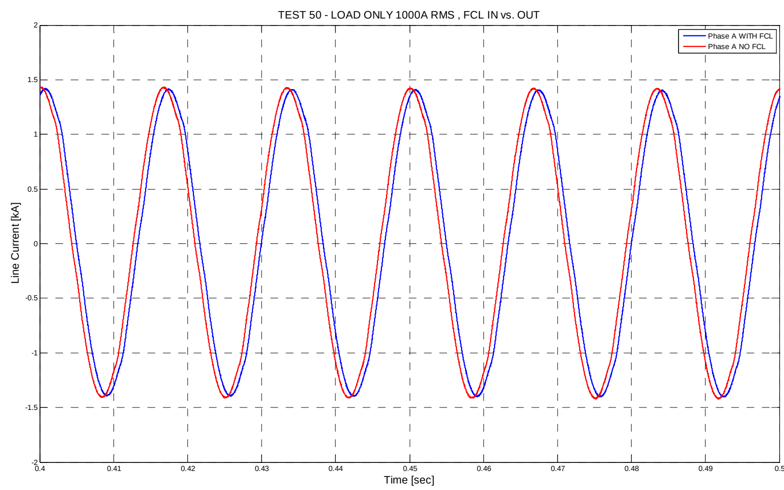


Figure A22: Line Current Ph A - 1000A FCL IN vs. OUT

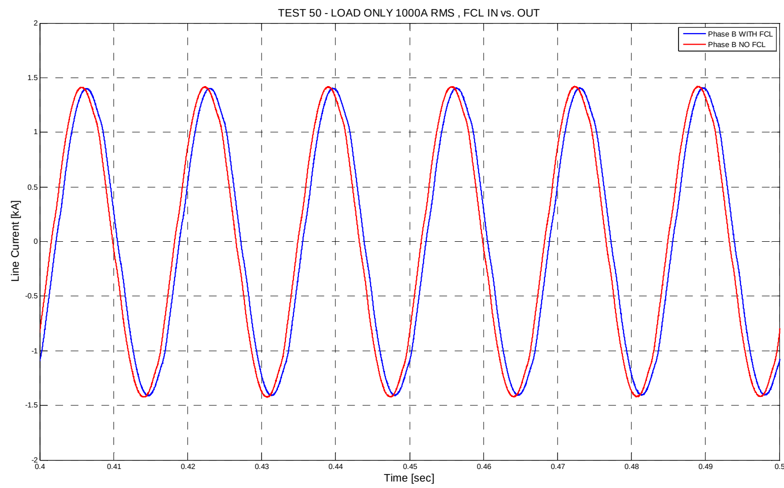


Figure A23: Line Current Ph B - 1000A FCL IN vs. OUT

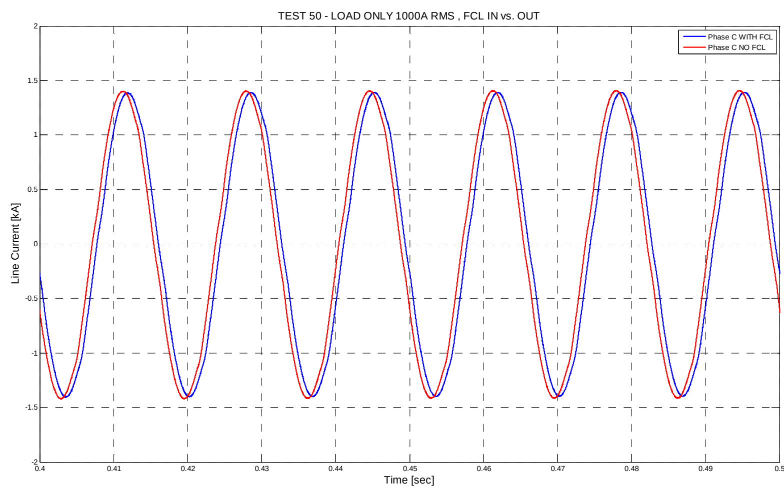


Figure A24: Line Current Ph C - 1000A FCL IN vs. OUT

8.9 TEST 51 - 1200 A RMS LOAD CURRENT NO FCL

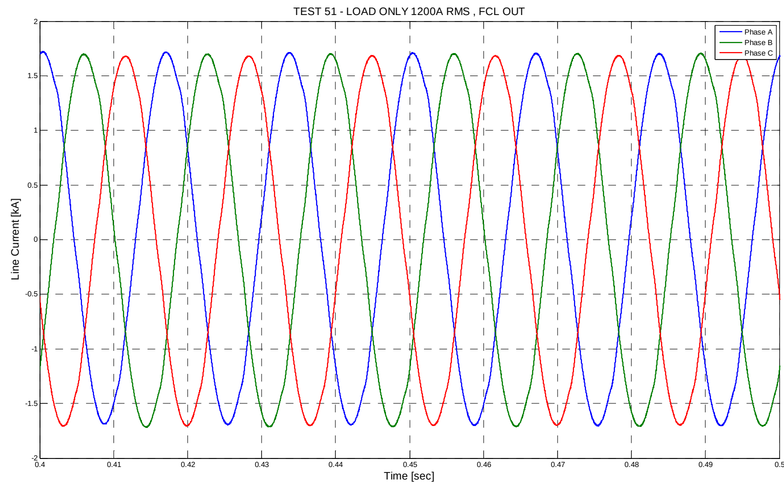


Figure A25: 1200A RMS load current – FCL Bypassed

8.10 TEST 53 - 1200 A RMS LOAD CURRENT

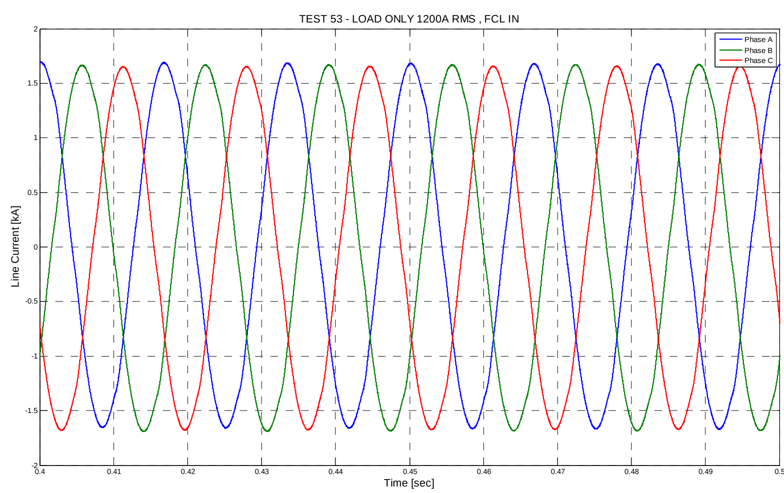


Figure A26: 1200A RMS load current – FCL IN

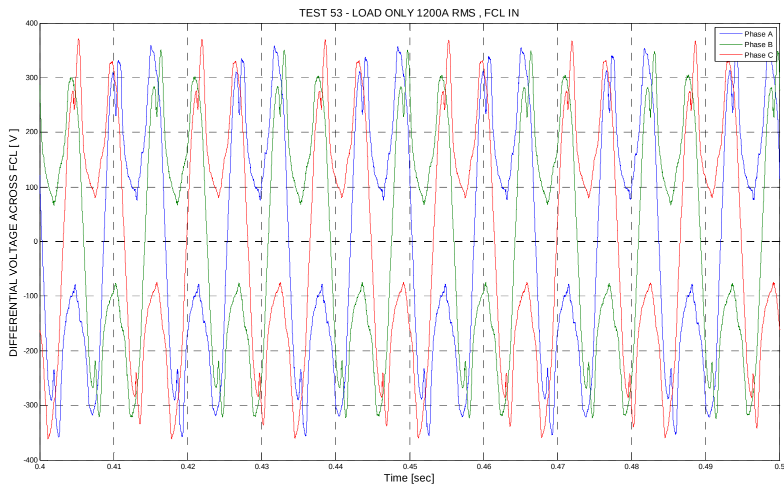


Figure A27: Voltage Drop at 1200A load current

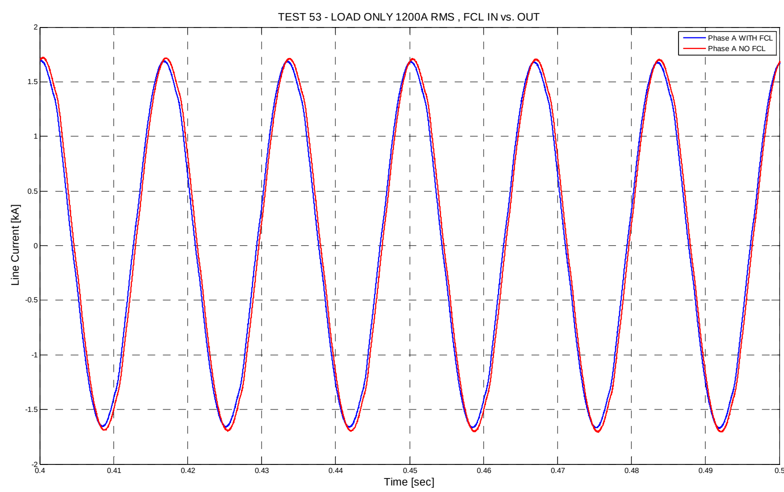


Figure A28: Line Current Ph A - 1200A FCL IN vs. OUT

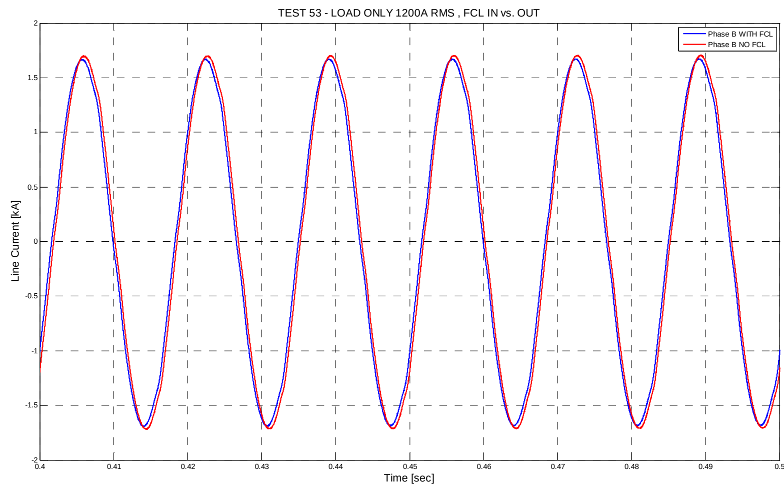


Figure A29: Line Current Ph B - 1200A FCL IN vs. OUT

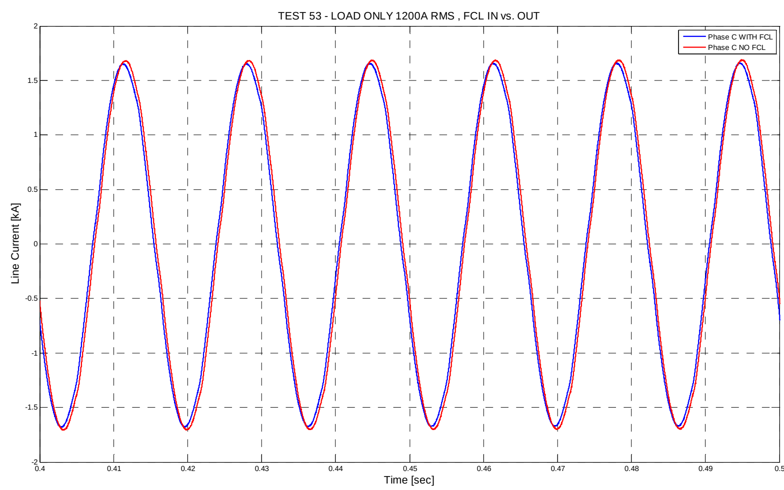


Figure A30: Line Current Ph C - 1200A FCL IN vs. OUT

8.11 TEST 54 - 1000 A RMS LOAD CURRENT, 142A DC BIAS

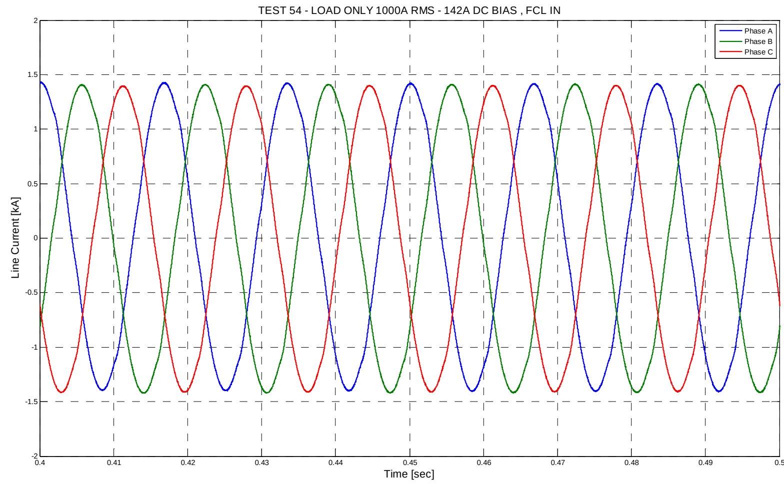


Figure A31: 1000A RMS load current – FCL IN – DC =142A

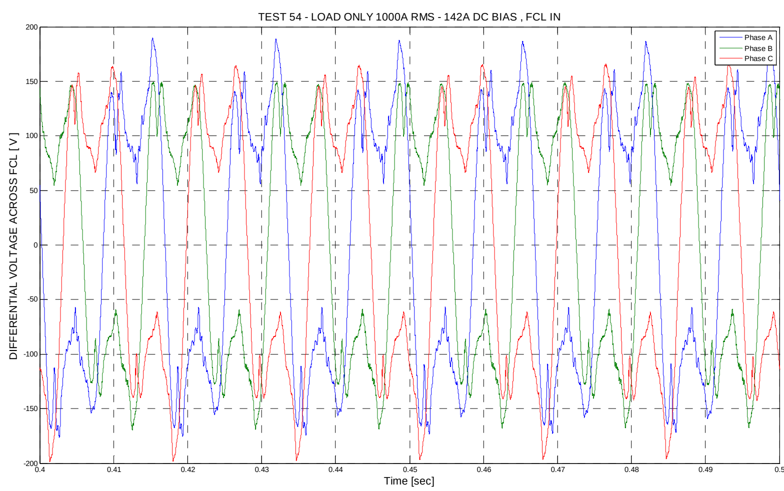


Figure A32: Voltage Drop at 1000A load current – DC 142A

8.12 TEST 55 - 1000 A RMS LOAD CURRENT, 160A DC BIAS

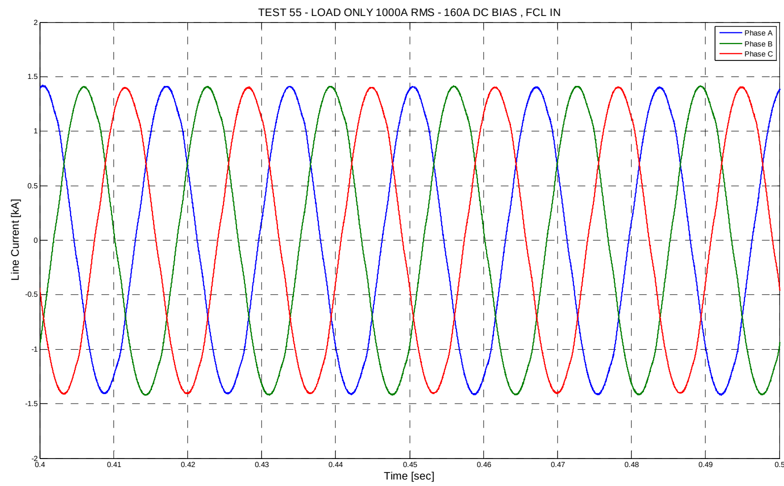


Figure A33: 1000A RMS load current – FCL IN – DC =160A

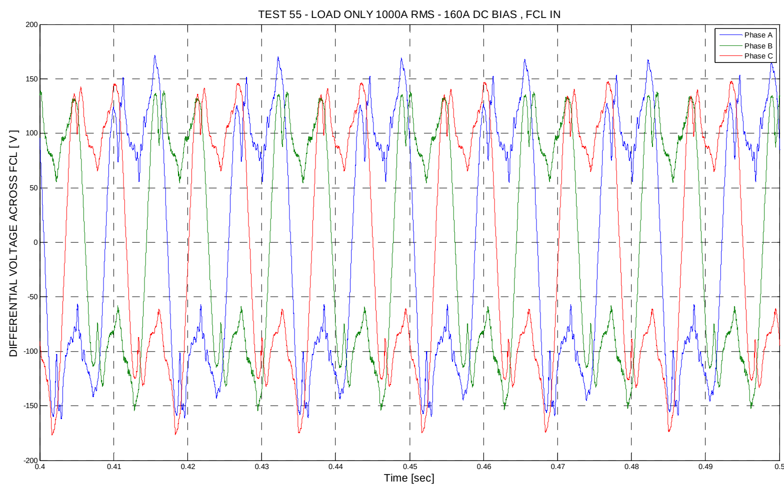


Figure A34: Voltage Drop at 1000A load current – DC 160A

8.13 TEST 50-54-55 - 1000 A RMS LOAD CURRENT, 100-142-160A DC BIAS

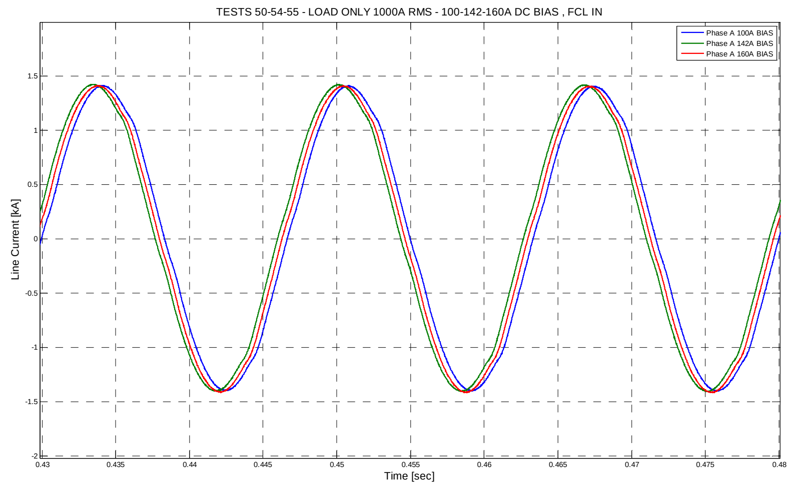


Figure A35: Line Current Ph A - 1000A AC, 100 -142 -160A DC

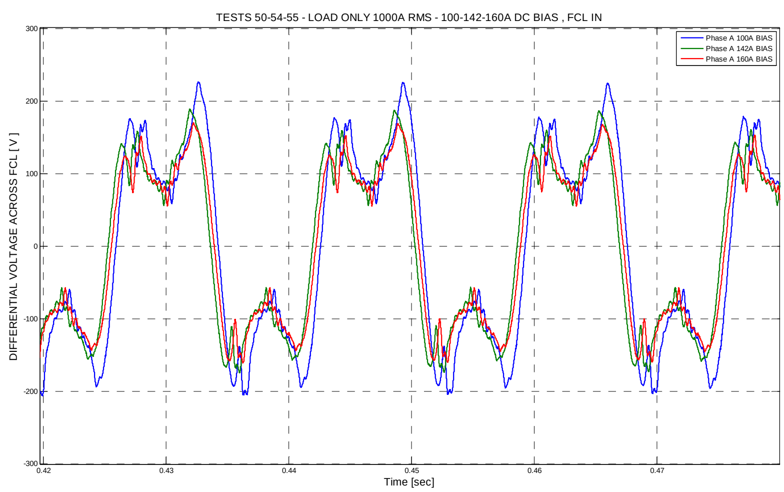


Figure A36: Voltage Drop Ph A - 1000A AC, 100 -142 -160A DC

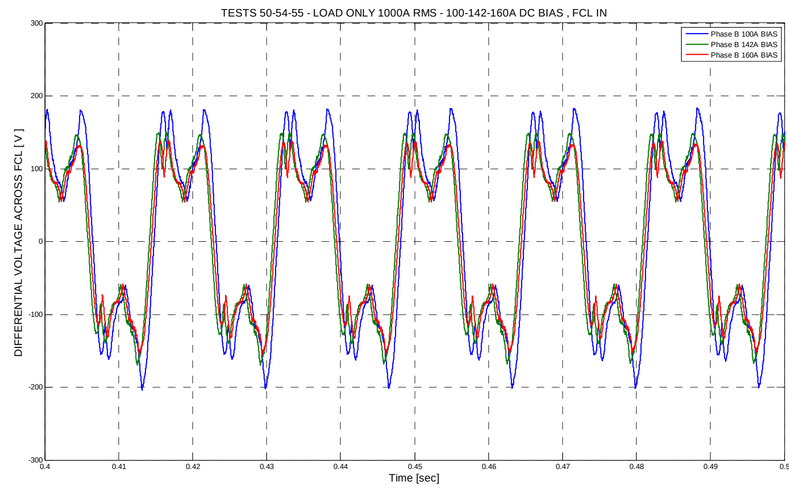


Figure A37: Voltage Drop Ph B - 1000A AC, 100 -142 -160A DC

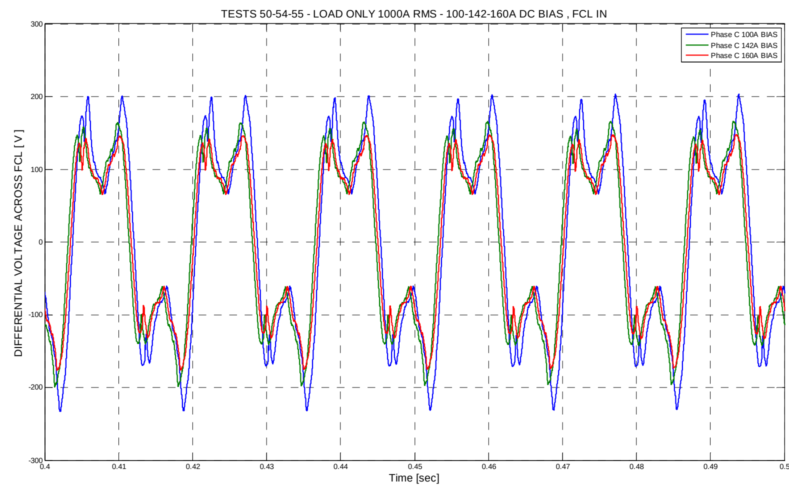


Figure A38: Voltage Drop Ph C - 1000A AC, 100 -142 -160A DC

9. APPENDIX B – FAULT CURRENT TESTS

9.1 Test 69 – Fault Characterization only 23kA, X/R=44

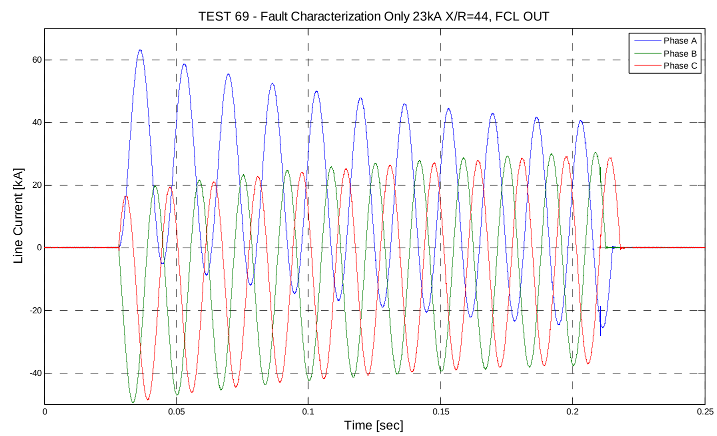


Figure B1: Fault characterization 23kA – FCL OUT

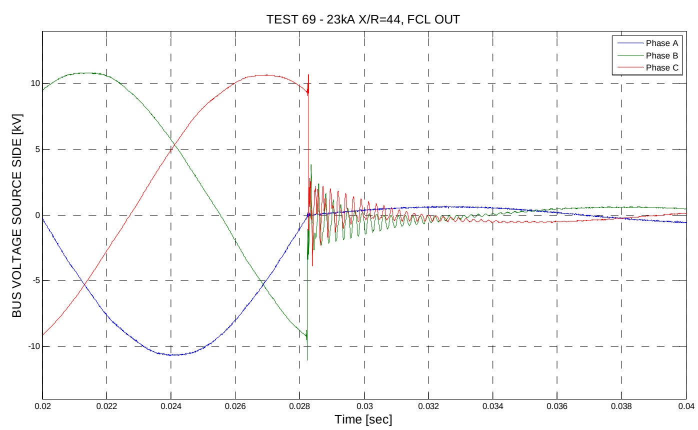


Figure B2: POW phase A- fault characterization 23kA – FCL OUT

9.2 Test 75 – 23kA Fault X/R=44

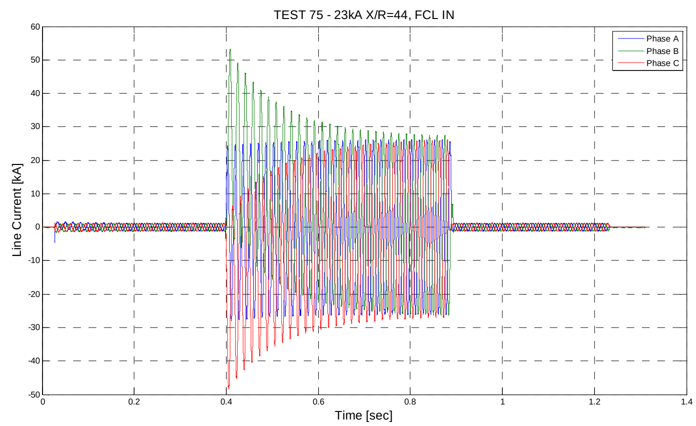


Figure B3: Fault current test- 23kA prospective – FCL IN

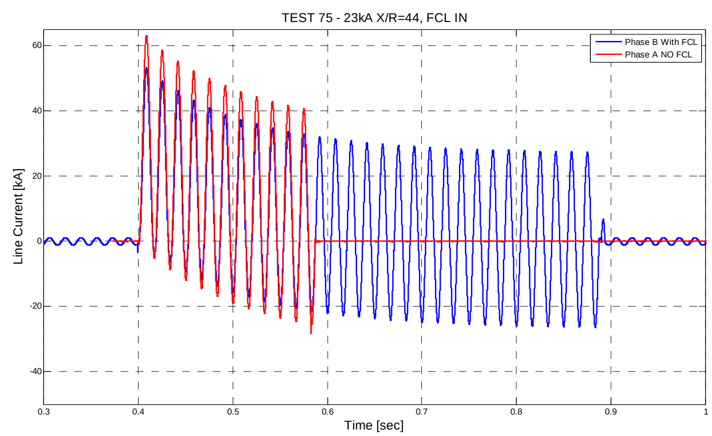


Figure B4: Single phase - 23kA prospective vs. clipped

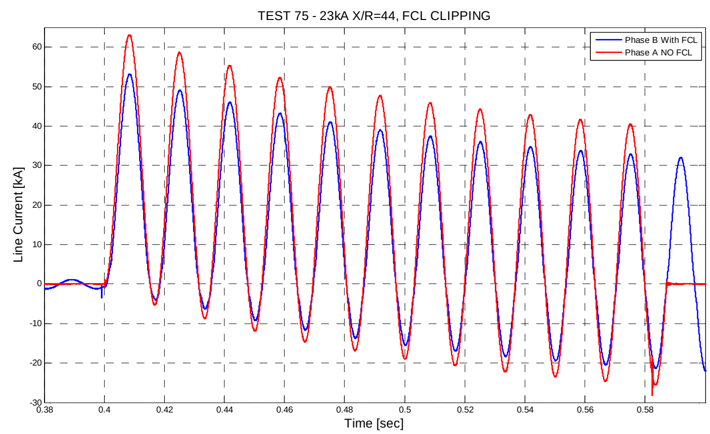


Figure B5: Single phase - 23kA prospective vs. clipped

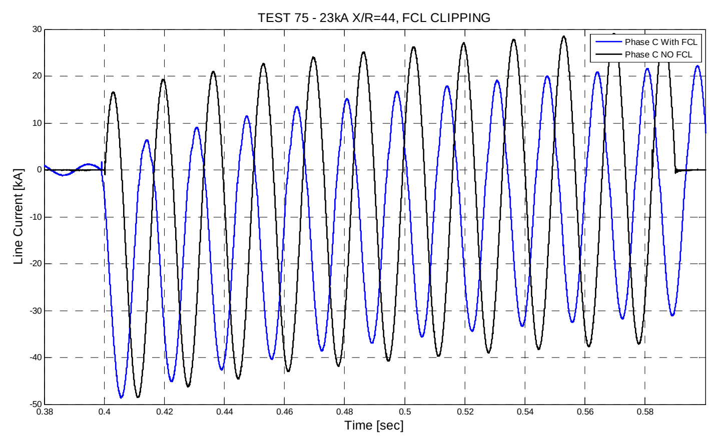


Figure B6: Phase C - 23kA prospective vs. clipped

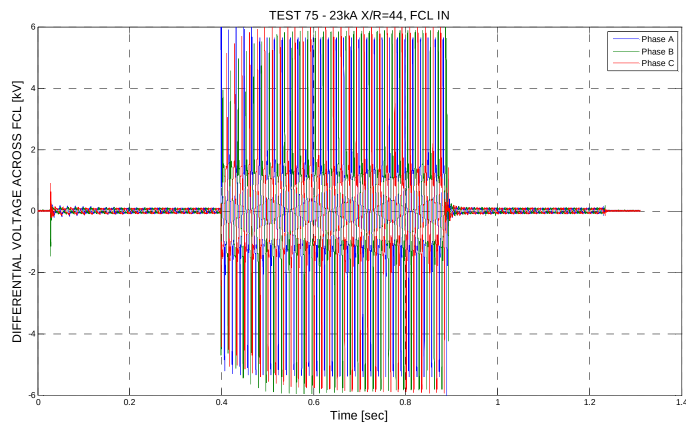


Figure B7: FCL Voltage - 23kA FCL IN

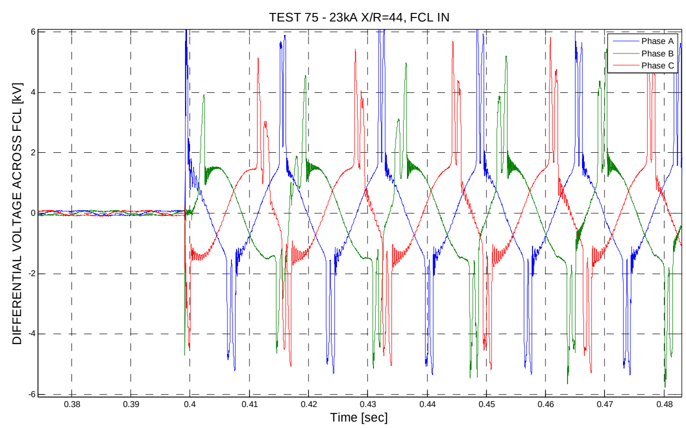


Figure B8: FCL Voltage - 23kA close up

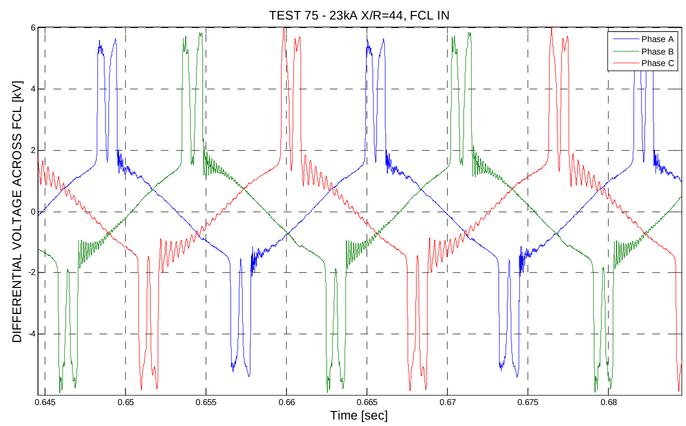


Figure B9: FCL Voltage - 23kA - zoom

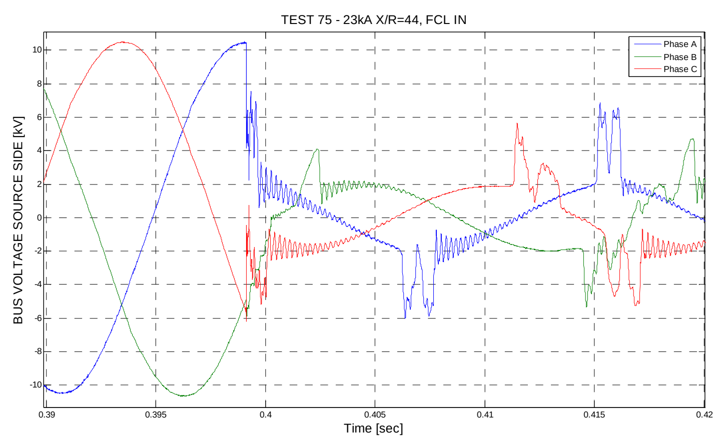


Figure B10: Source Voltage - 23kA - POW

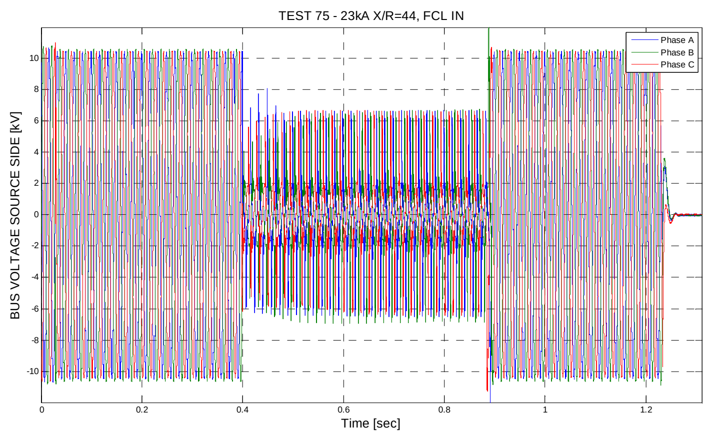


Figure B11: Source Voltage - 23kA

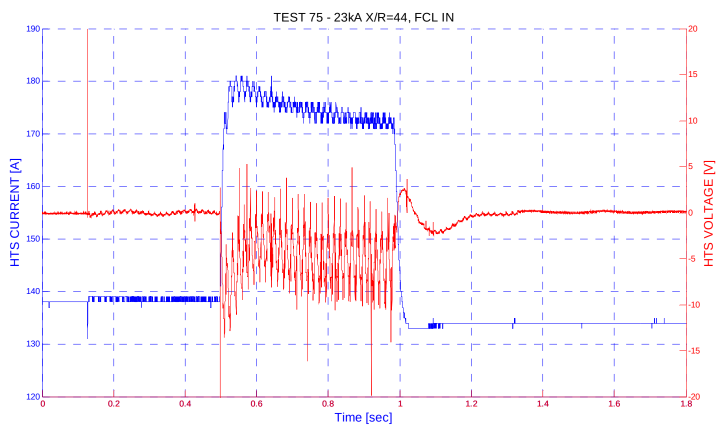


Figure B12: HTS coil Voltage and Current - 23kA

9.3 Test 68 – Fault Characterization only 20kA, X/R=21.6

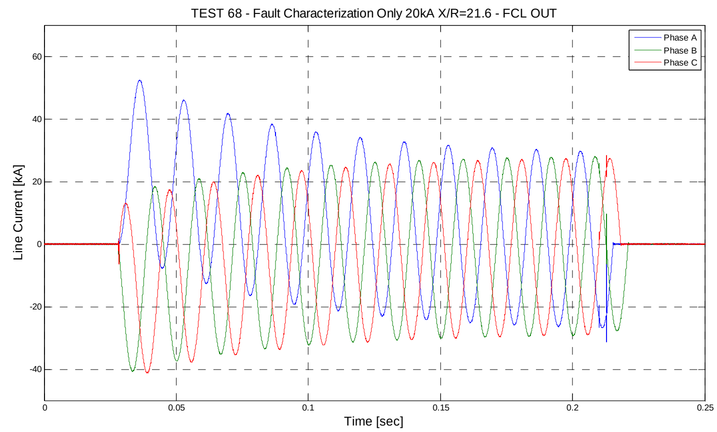


Figure B13: Fault characterization 20kA – FCL OUT

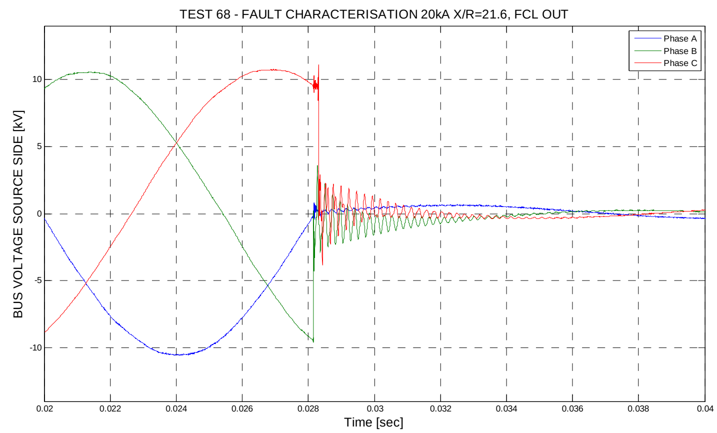


Figure B14: POW phase A- fault characterization 20kA – FCL OUT

9.4 Test 71 – 20kA Fault X/R=21.6

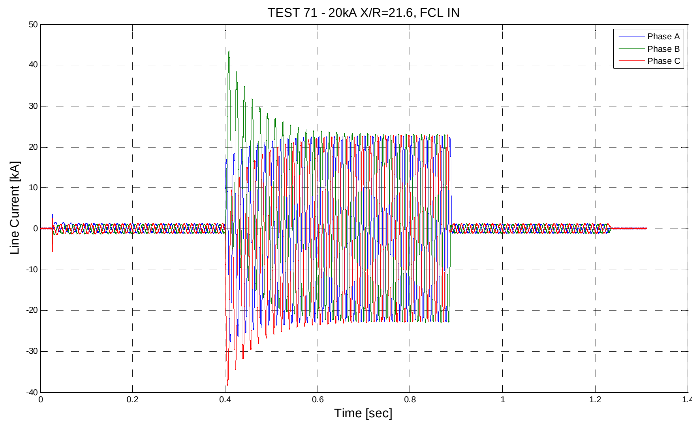


Figure B15: Fault current test- 20kA prospective – FCL IN

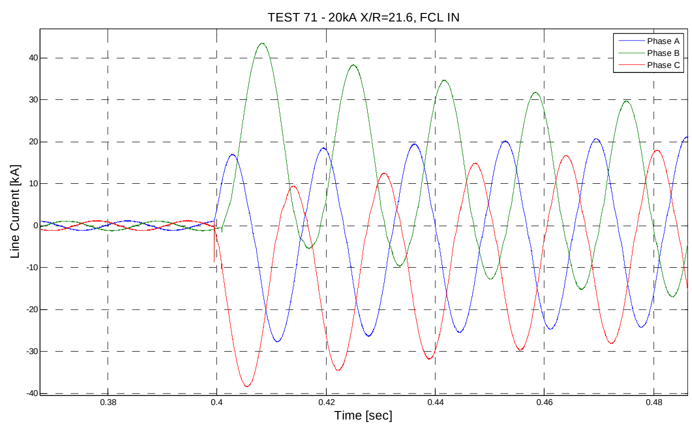


Figure B16: Fault current test- 20kA prospective – FCL IN

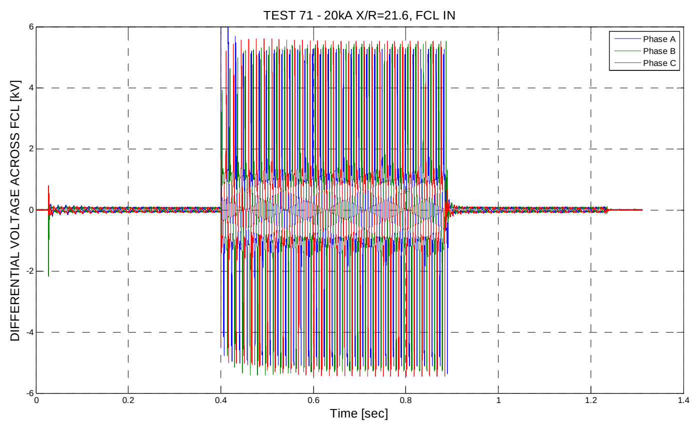


Figure B17: FCL Voltage - 20kA FCL IN

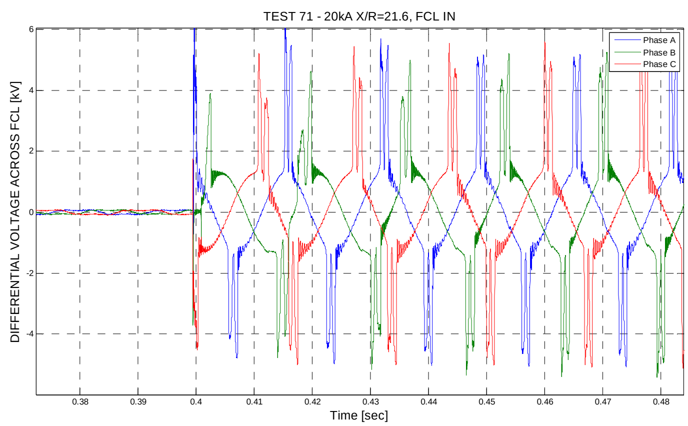


Figure B18: FCL Voltage - 20kA close up

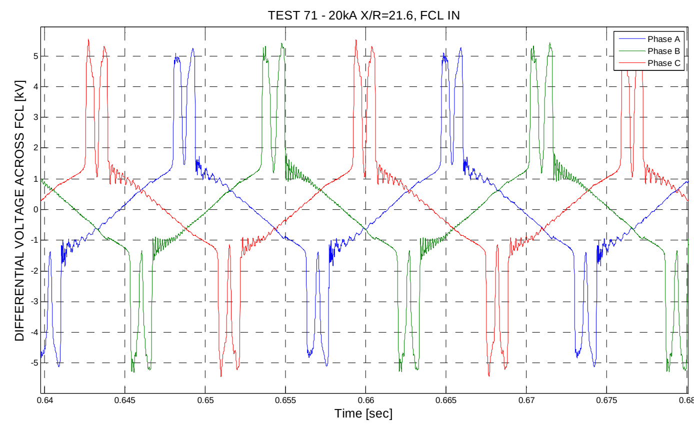


Figure B19: FCL Voltage - 20kA - zoom

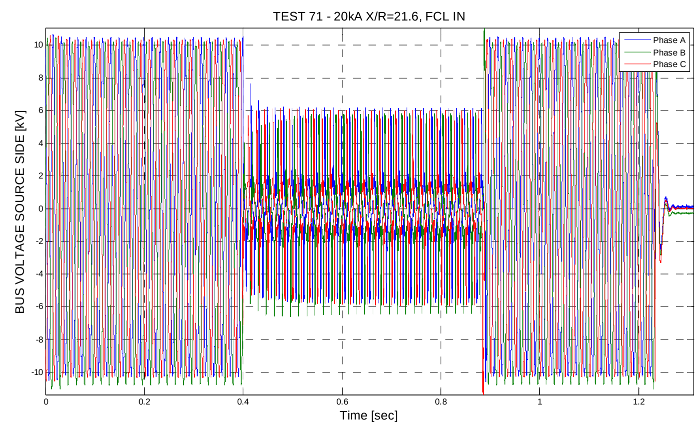


Figure B20: Source Voltage - 20kA

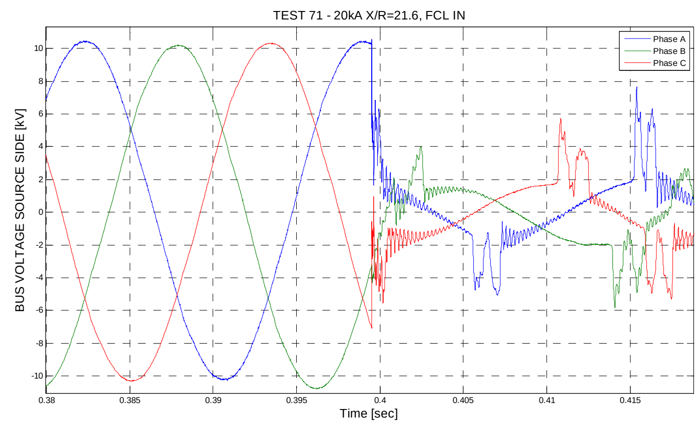


Figure B21: Source Voltage - 20kA - POW

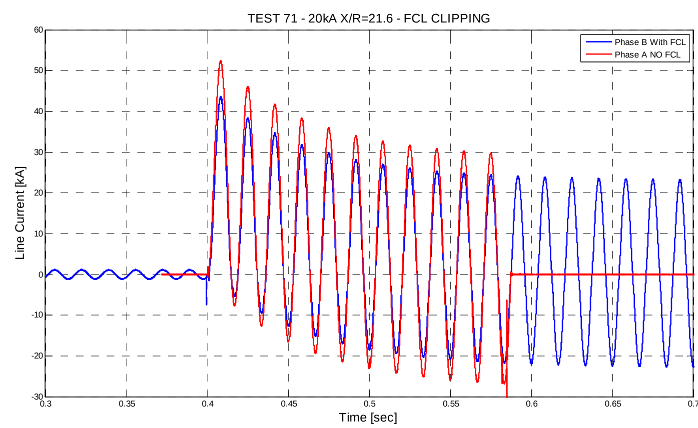


Figure B22: Single phase - 20kA prospective vs. clipped

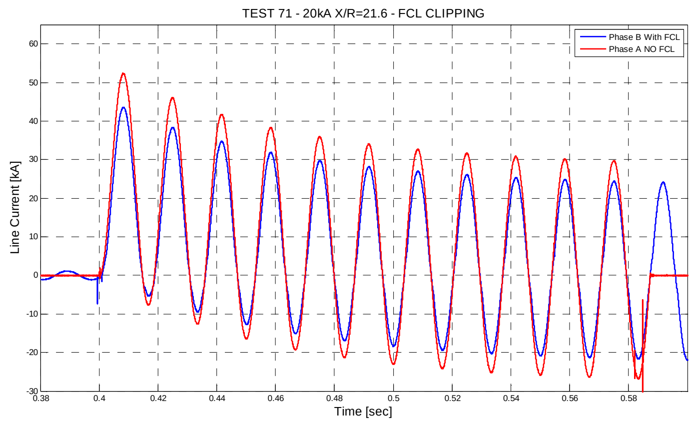


Figure B23: Single phase - 20kA prospective vs. clipped

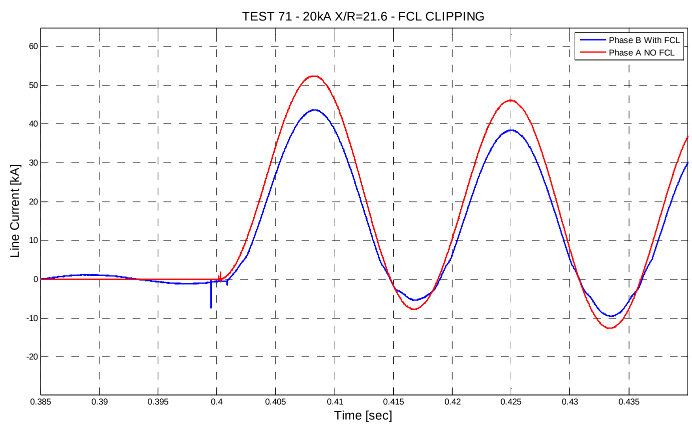


Figure B24: Single phase - 20kA prospective vs. clipped

9.5 Test 67 – Fault Characterization only 15kA, X/R=26.3

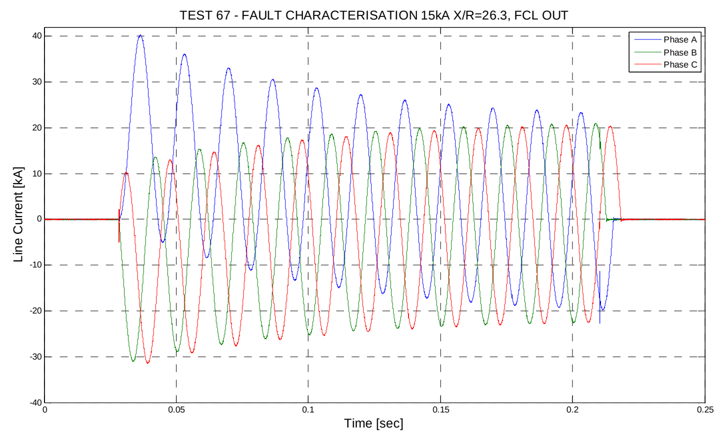


Figure B25: Fault characterization 15kA – FCL OUT

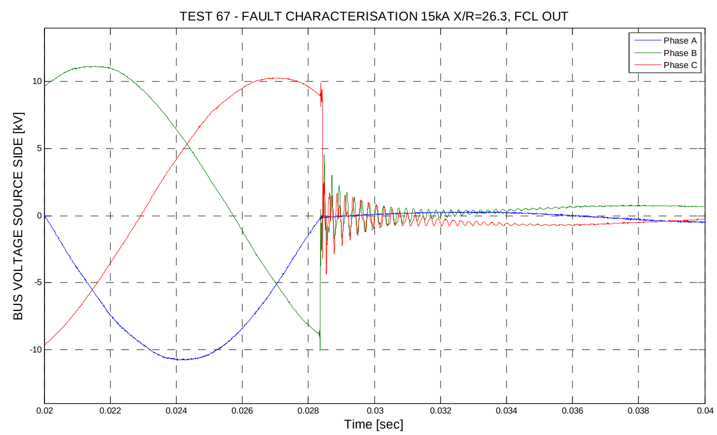


Figure B26: POW phase A- fault characterization 15kA – FCL OUT

9.6 Test 70 – 15kA Fault X/R=26.3

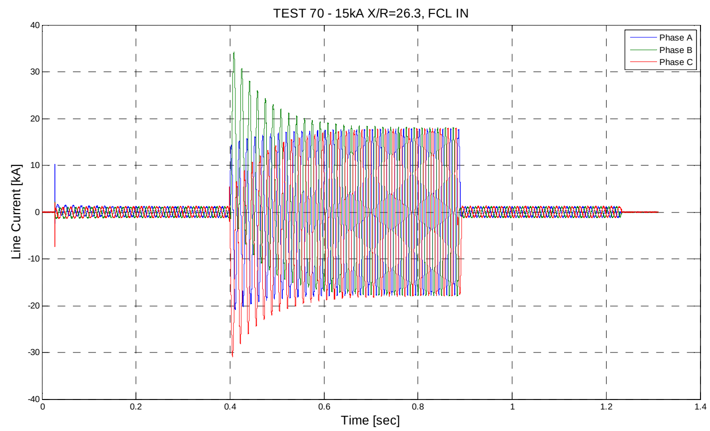


Figure B27: Fault current test- 15kA prospective – FCL IN

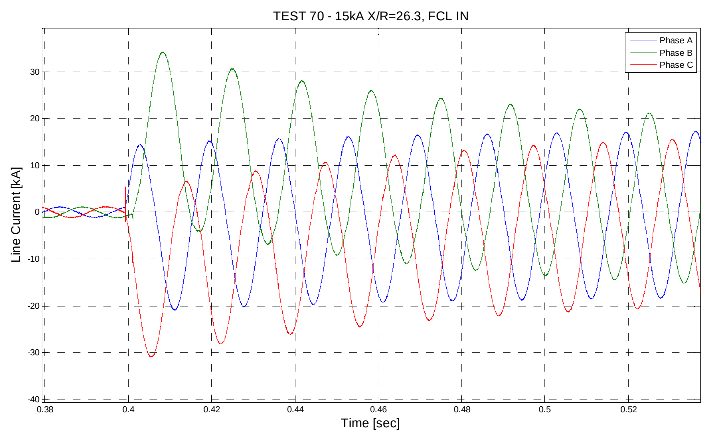


Figure B28: Fault current test- 15kA prospective – FCL IN

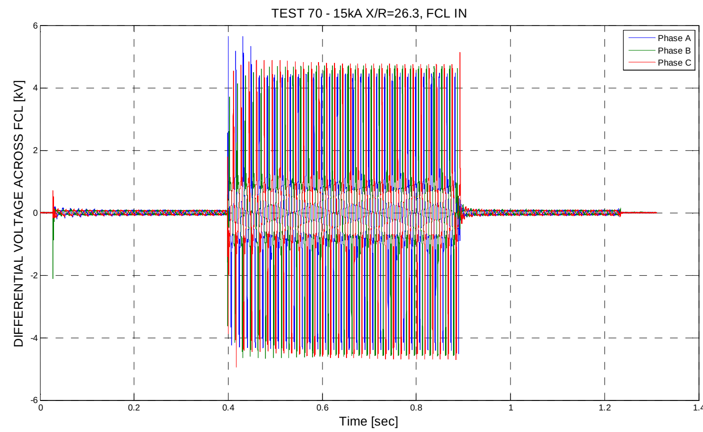


Figure B29: FCL Voltage - 15kA FCL IN

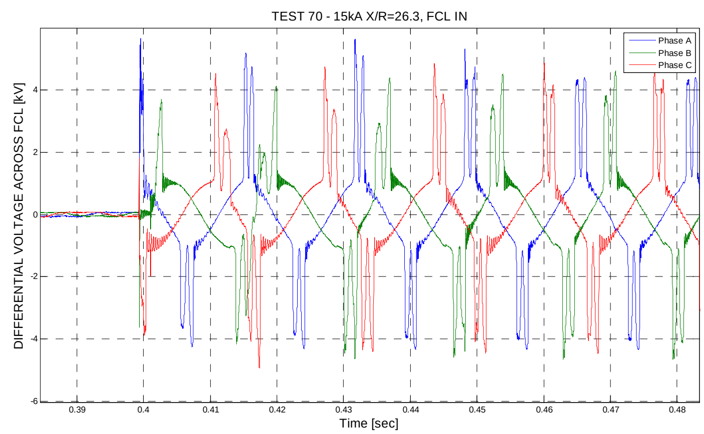


Figure B30: FCL Voltage - 15kA FCL IN close up

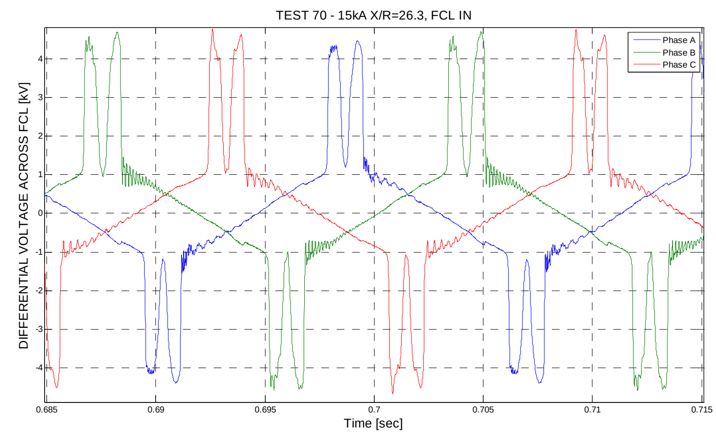


Figure B31: FCL Voltage - 15kA FCL IN zoom

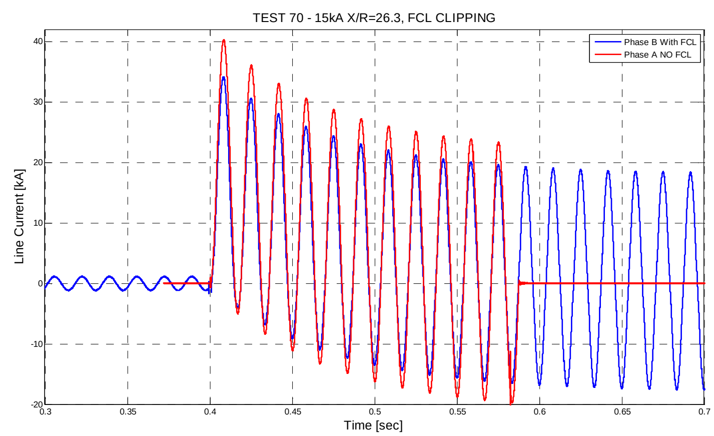


Figure B32: Single phase - 15kA prospective vs. clipped

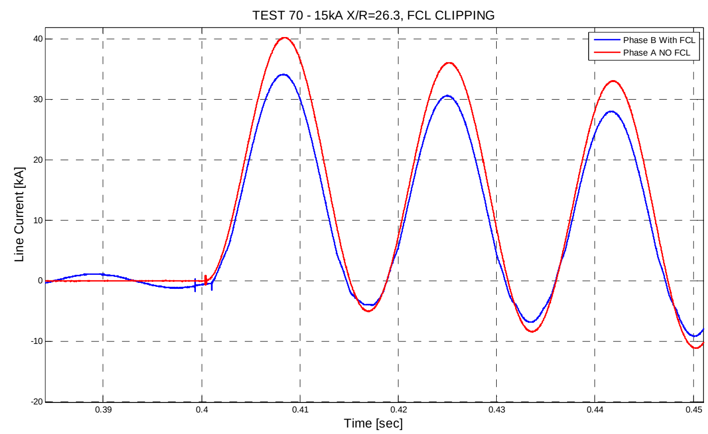


Figure B33: Single phase - 15kA prospective vs. clipped

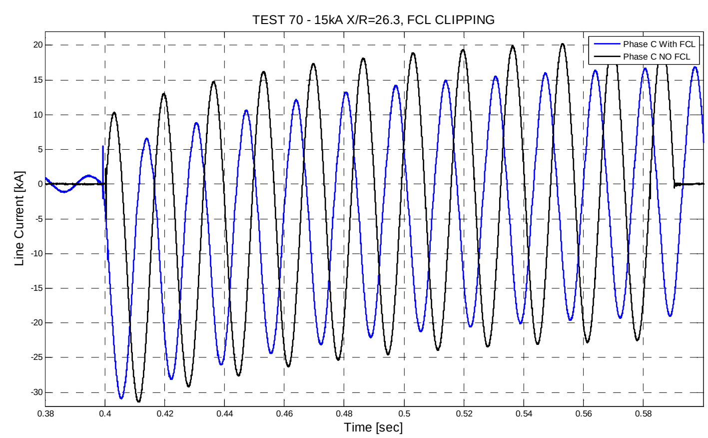


Figure B34: Phase C - 15kA prospective vs. clipped

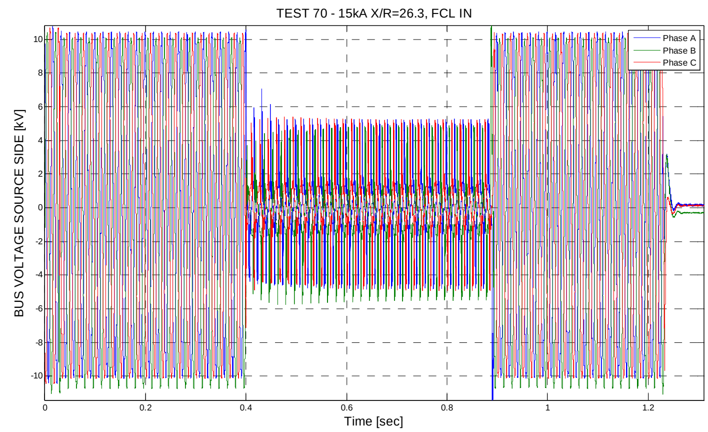


Figure B35: Source Voltage - 15kA

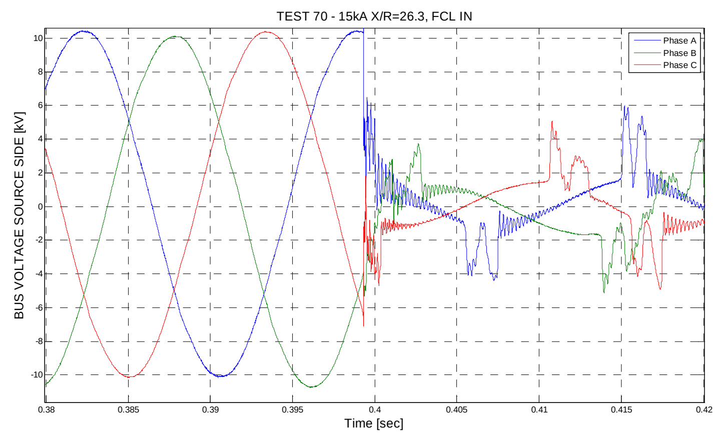


Figure B36: Source Voltage - 15kA - POW

9.7 Test 64 – Fault Characterization only 12.5kA, X/R=19.7

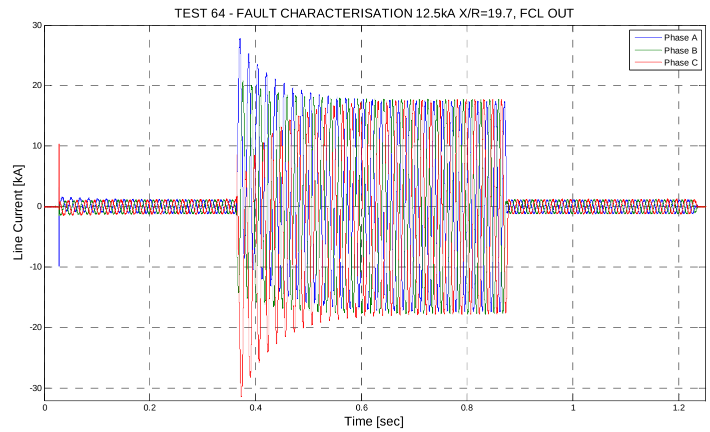


Figure B37: Fault characterization 12.5kA – FCL OUT

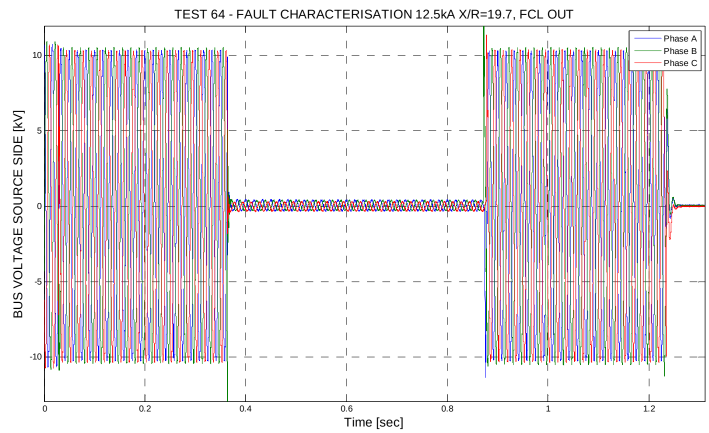


Figure B38: Source voltage - Fault characterization 12.5kA

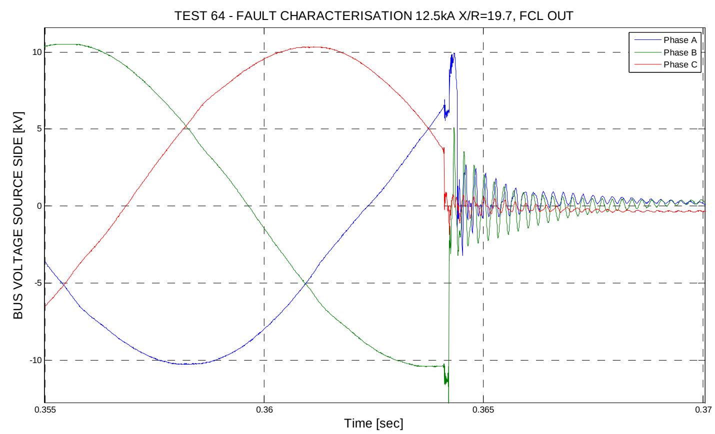


Figure B39: POW phase A- fault characterization 12.5kA

9.8 Test 65 – 12.5kA Fault X/R=19.7

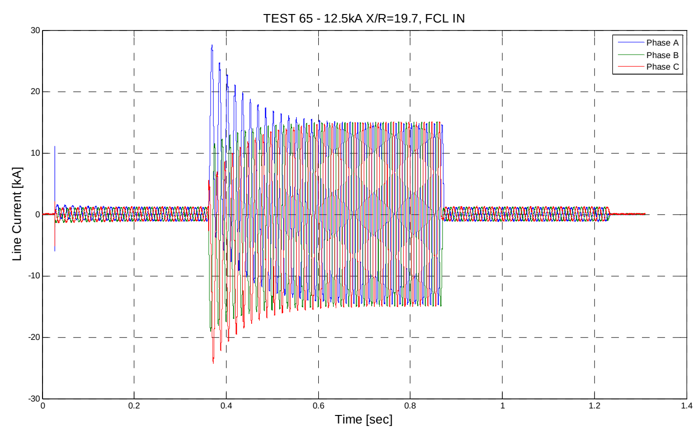


Figure B40: Fault current test- 12.5kA prospective – FCL IN

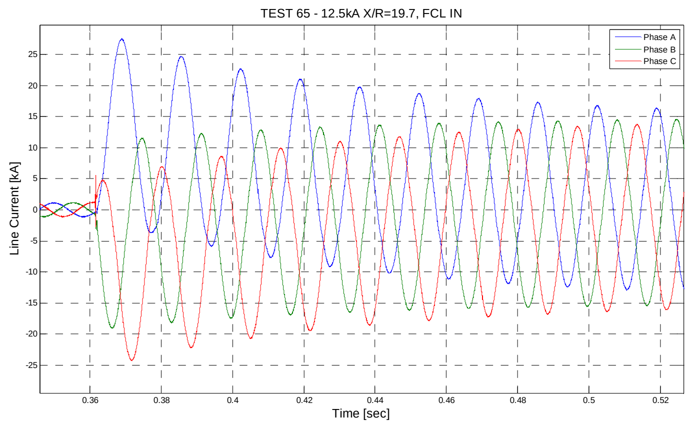


Figure B41: Fault current test- 12.5kA prospective – FCL IN

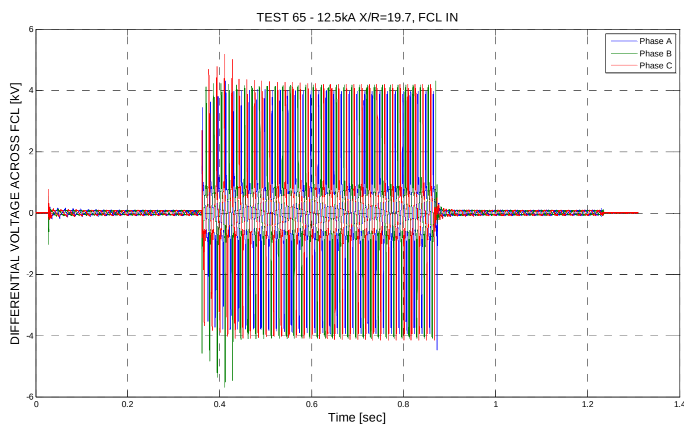


Figure B42: FCL Voltage – 12.5kA FCL IN

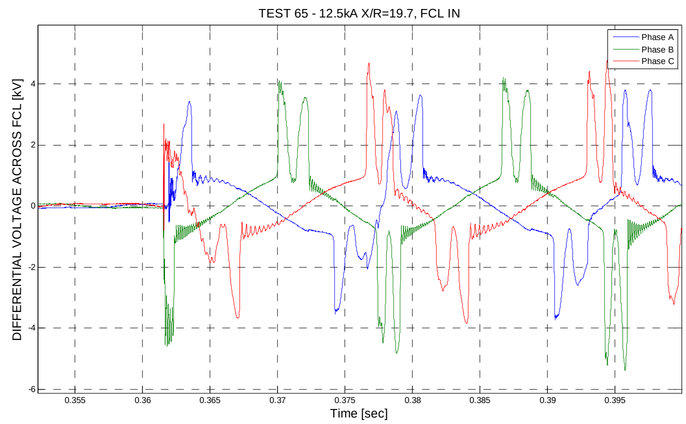


Figure B43: FCL Voltage – 12.5kA FCL IN close up

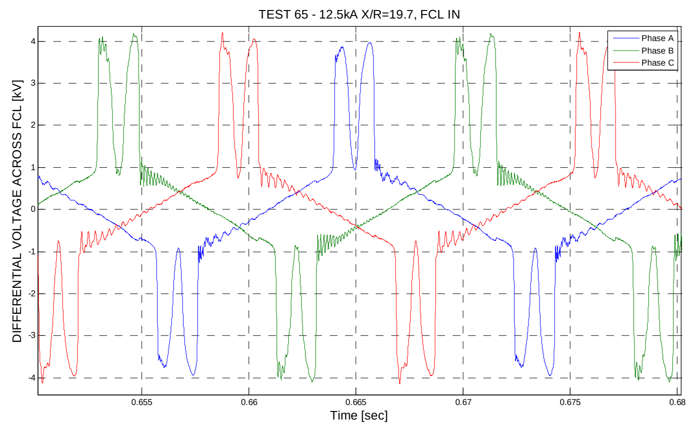


Figure B44: FCL Voltage – 12.5kA FCL IN zoom

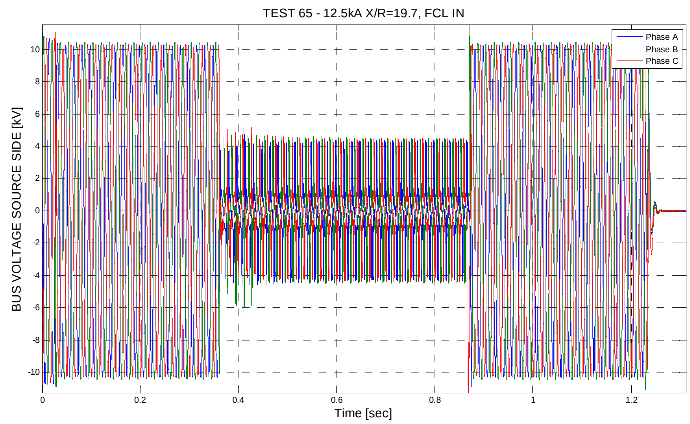


Figure B45: Source Voltage – 12.5kA

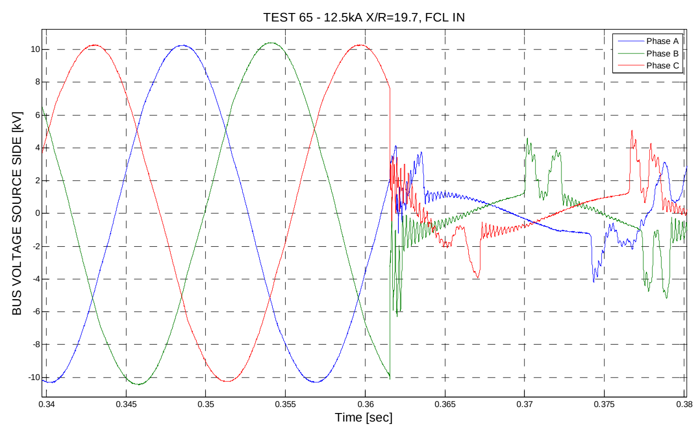


Figure B46: Source Voltage – 12.5kA - POW

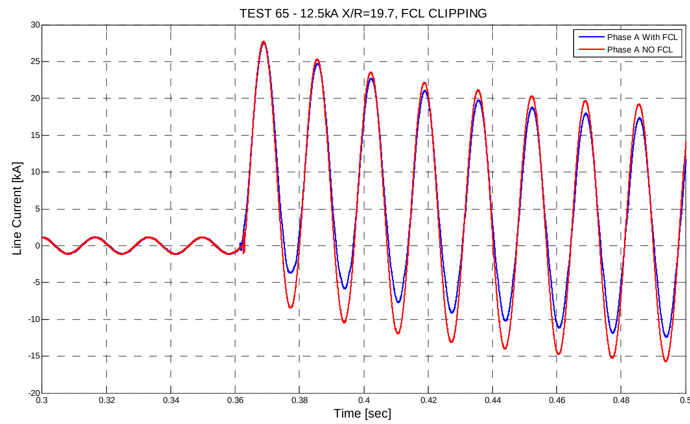


Figure B47: Single phase – 12.5kA prospective vs. clipped

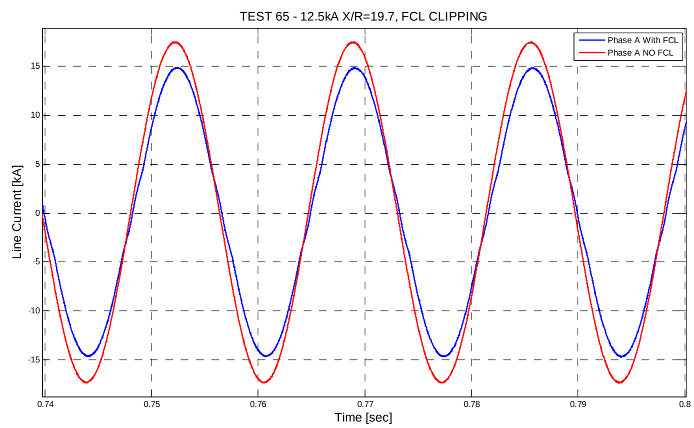


Figure B48: Single phase – 12.5kA prospective vs. clipped

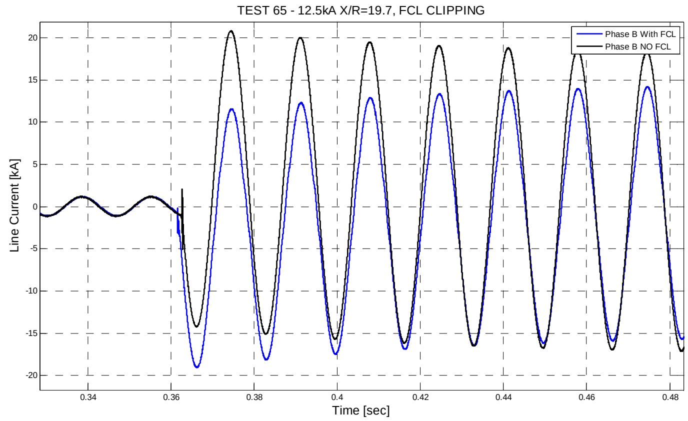


Figure B49: Phase B – 12.5kA prospective vs. clipped

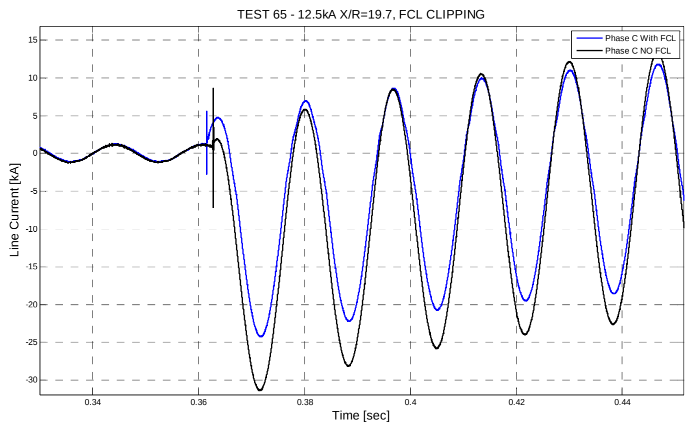


Figure B50: Phase C – 12.5kA prospective vs. clipped

9.9 Test 62 – Fault Characterization only, 8kA, X/R=19.8

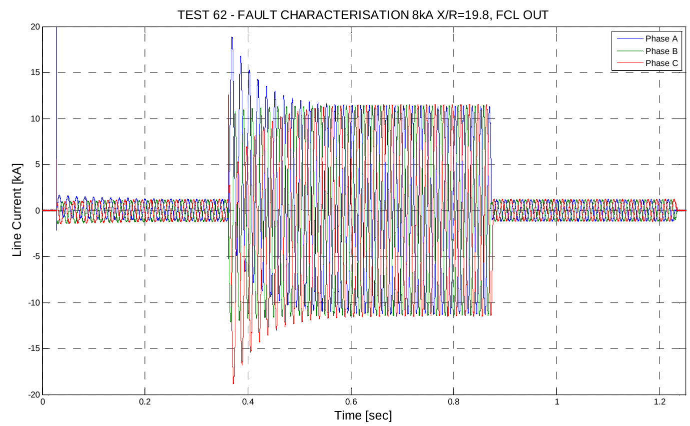


Figure B51: Fault characterization 8kA – FCL OUT

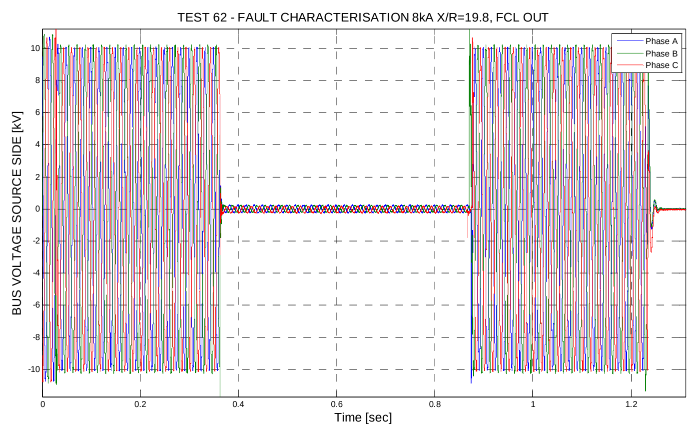


Figure B52: Source voltage - Fault characterization 8kA

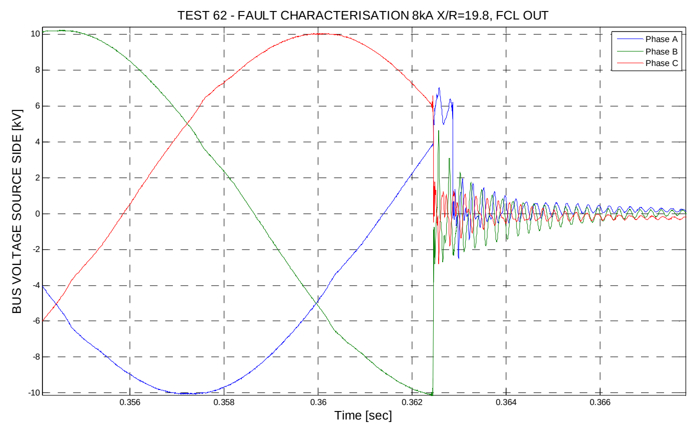


Figure B53: POW phase A- fault characterization 8kA

9.10 Test 63 – 8kA Fault X/R=19.8

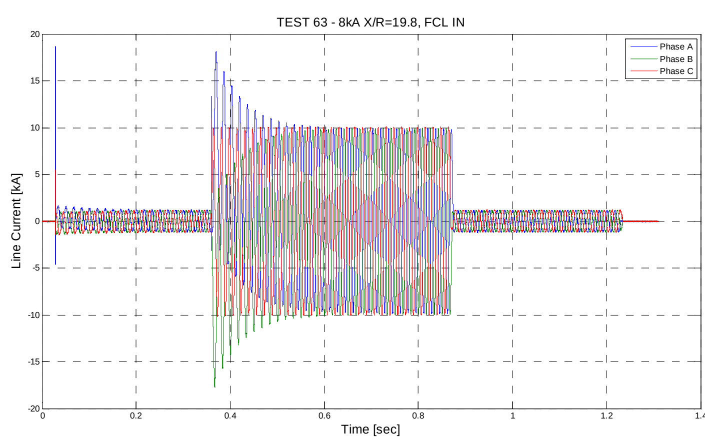


Figure B54: Fault current test- 8kA prospective – FCL IN

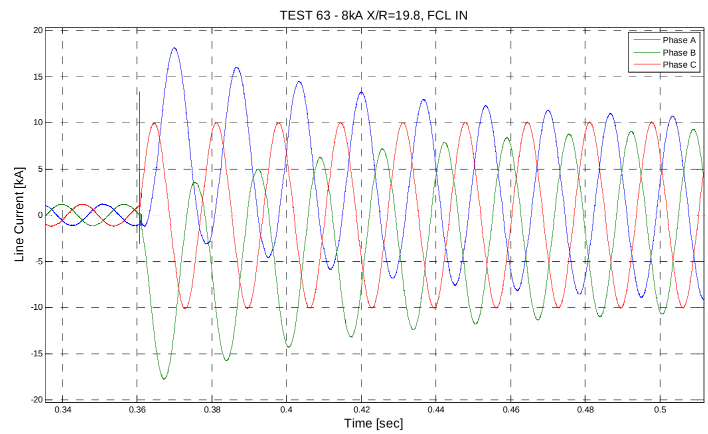


Figure B55: Fault current test- 8kA prospective – FCL IN

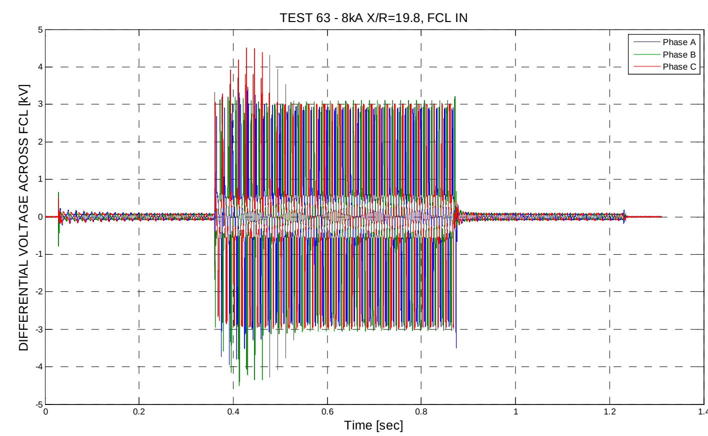


Figure B56: FCL Voltage – 8kA FCL IN

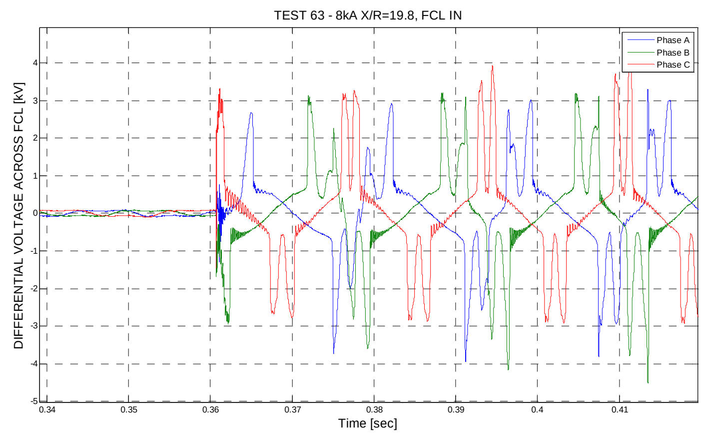


Figure B57: FCL Voltage – 8kA FCL IN close up

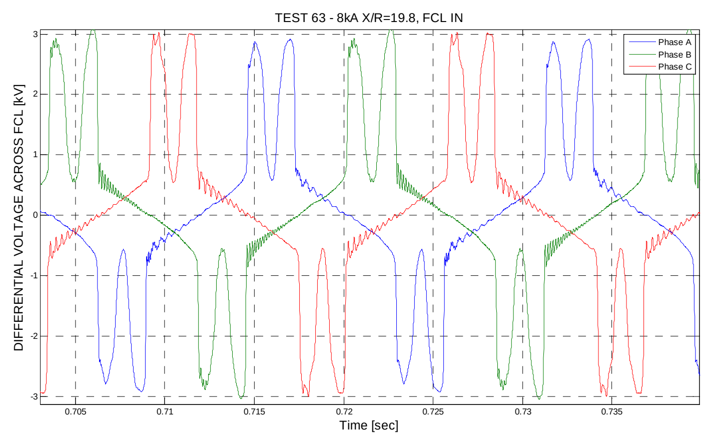


Figure B58: FCL Voltage – 8kA FCL IN zoom

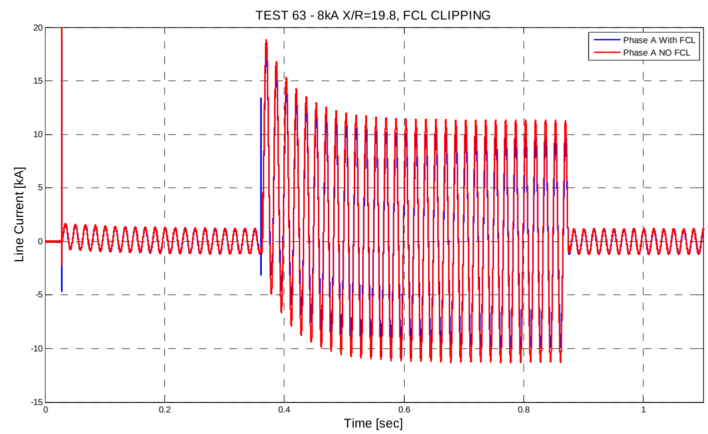


Figure B59: Single phase – 8kA prospective vs. clipped

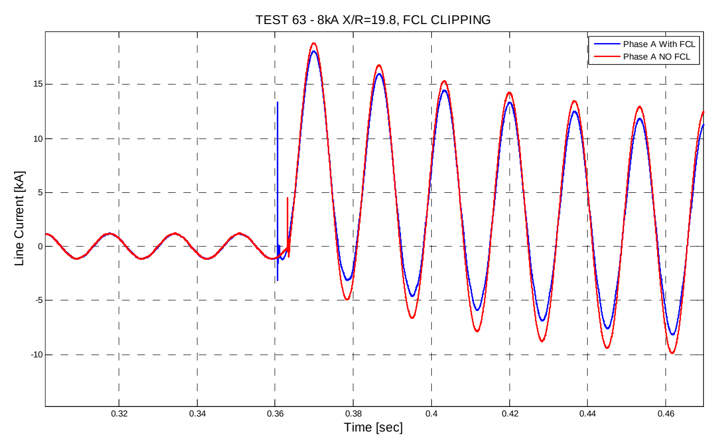


Figure B60: Phase A – 8kA prospective vs. clipped

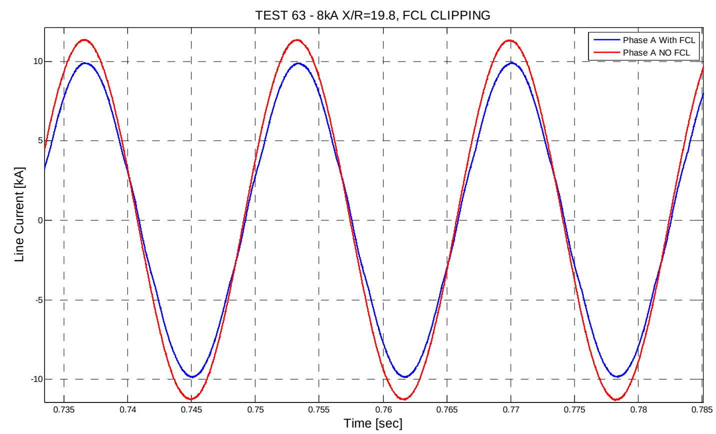


Figure B61: Phase A – 8kA prospective vs. clipped

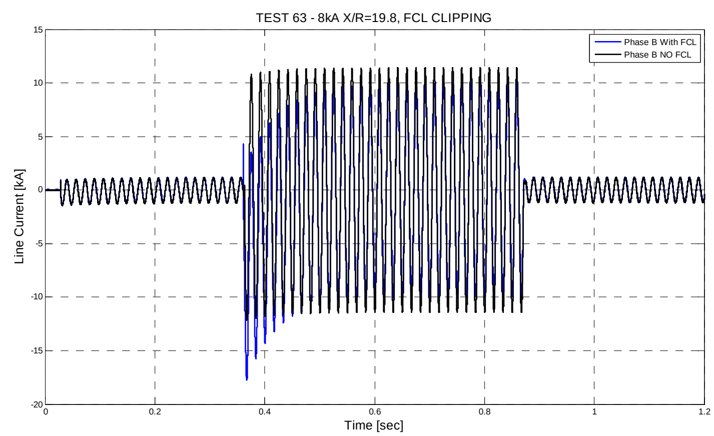


Figure B62: Phase B – 8kA prospective vs. clipped

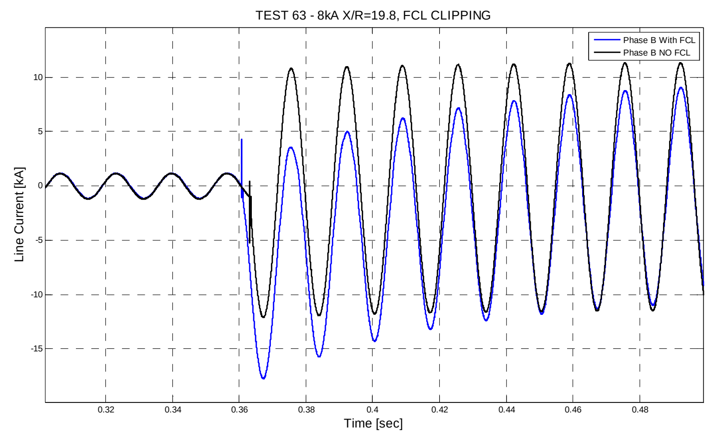


Figure B63: Phase B – 8kA prospective vs. clipped

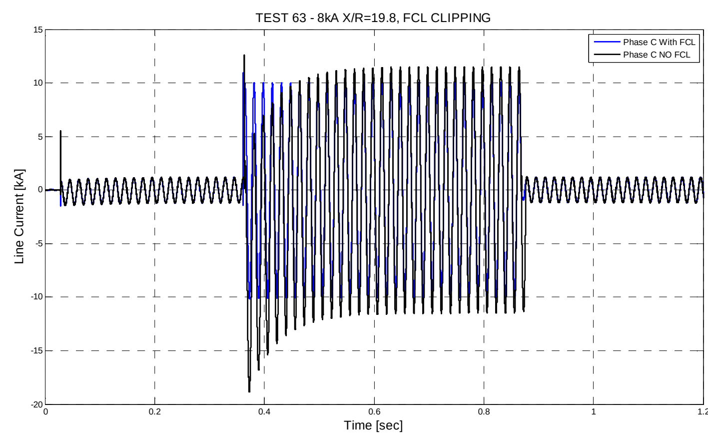


Figure B64: Phase C – 8kA prospective vs. clipped

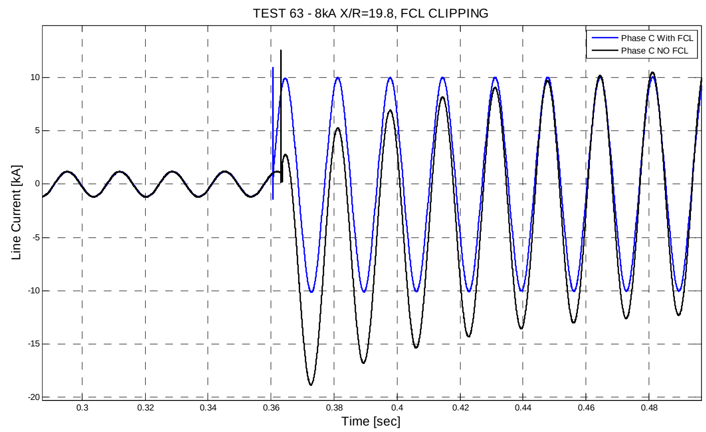


Figure B65: Phase C – 8kA prospective vs. clipped

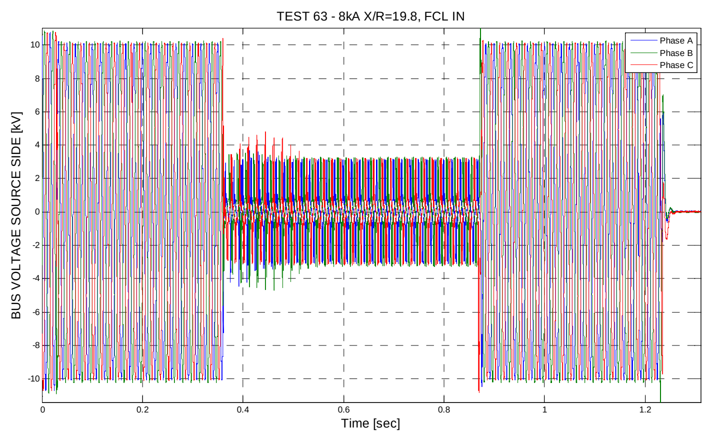


Figure B66: Source Voltage – 8kA

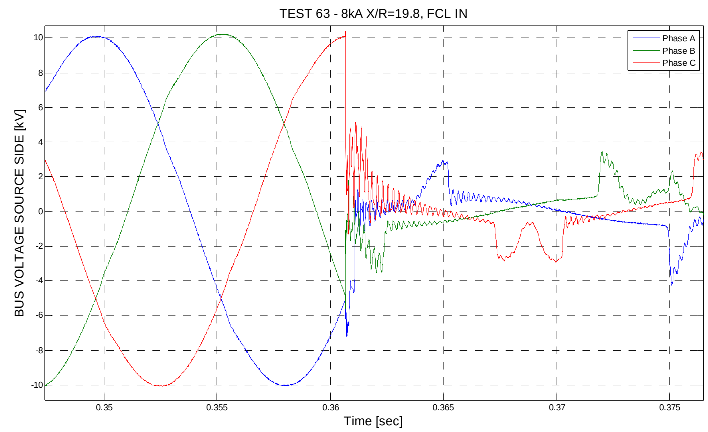


Figure B67: Source Voltage – 8kA - POW

9.11 Test 60 – Fault Characterization only, 3kA, X/R=22.9

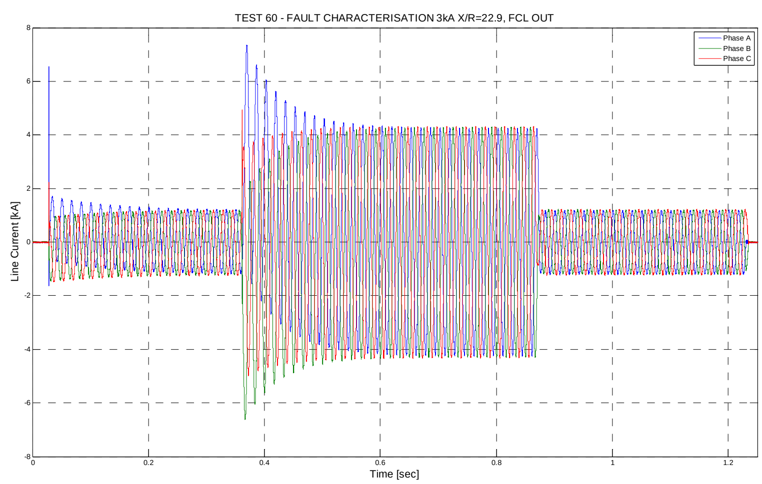


Figure B68: Fault characterization 3kA – FCL OUT

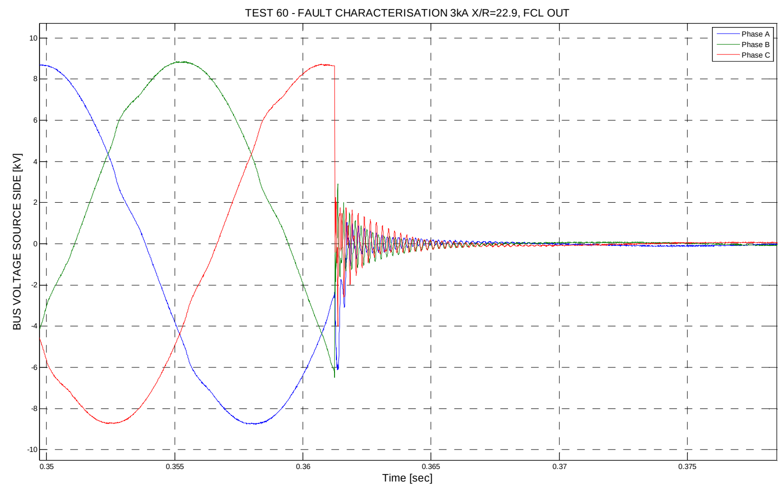


Figure B69: POW phase A- fault characterization 3kA

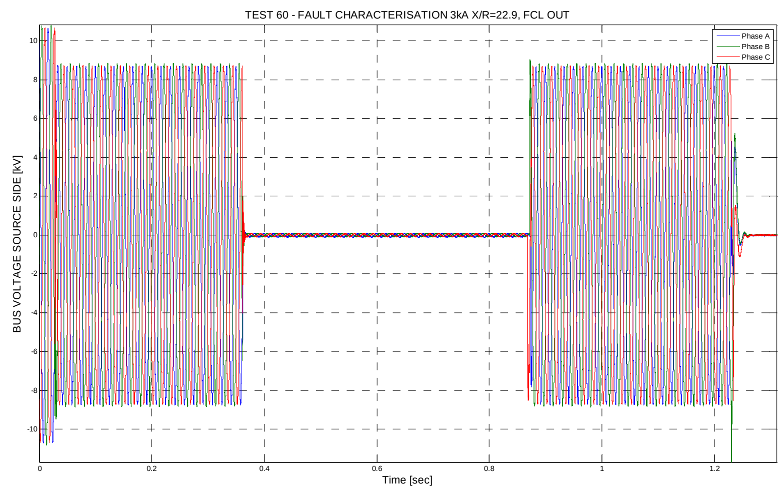


Figure B70: Source voltage - Fault characterization 3kA

9.12 Test 61 – 3kA Fault X/R=22.9

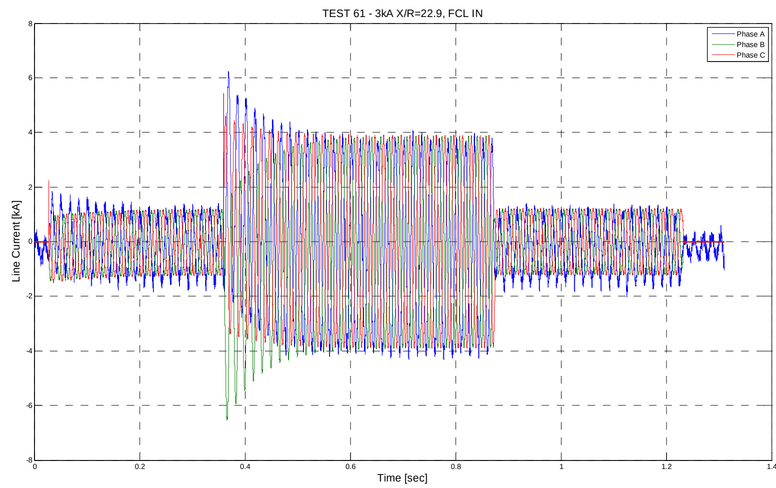


Figure B71: Fault current test- 3kA prospective – FCL IN

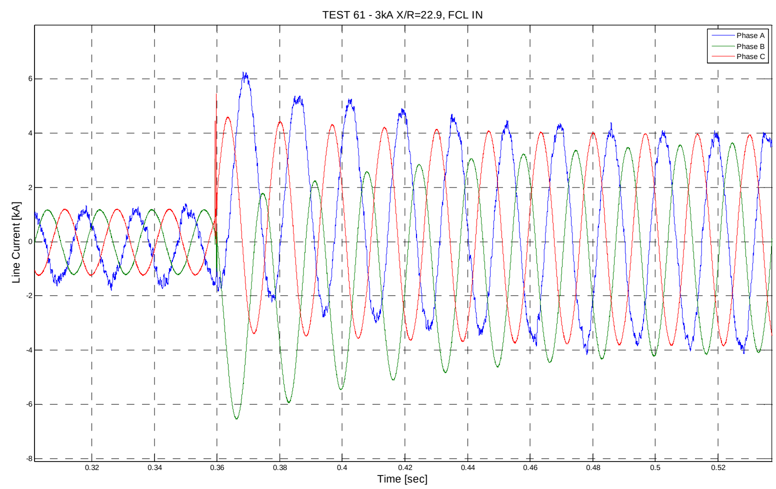


Figure B72: Fault current test- 3kA prospective – FCL IN

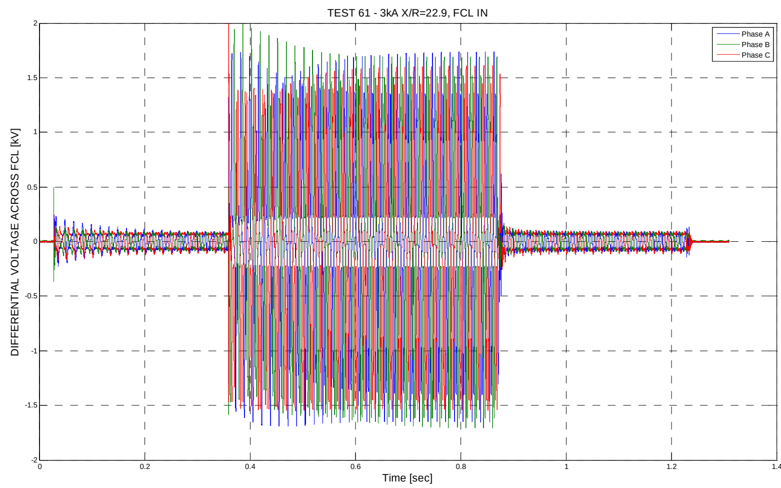


Figure B73: FCL Voltage – 3kA FCL IN

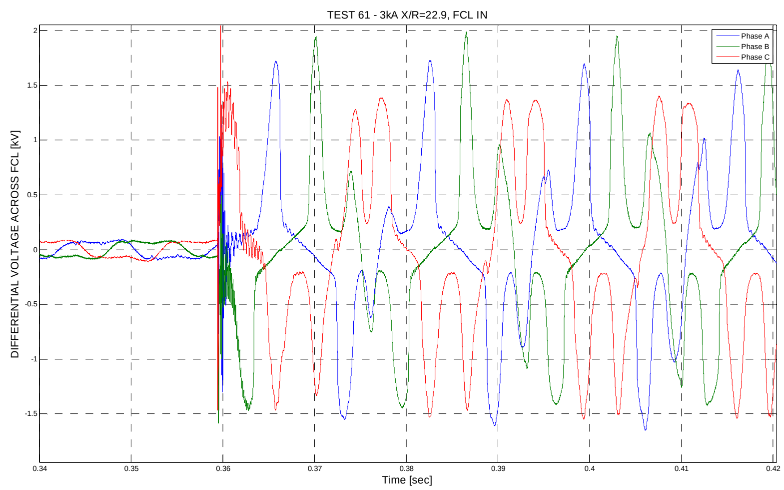


Figure B74: FCL Voltage – 3kA FCL IN close up

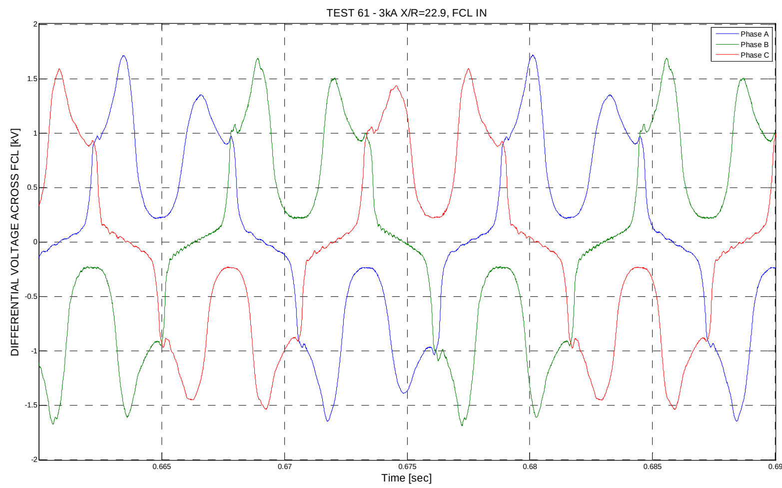


Figure B75: FCL Voltage – 3kA FCL IN zoom

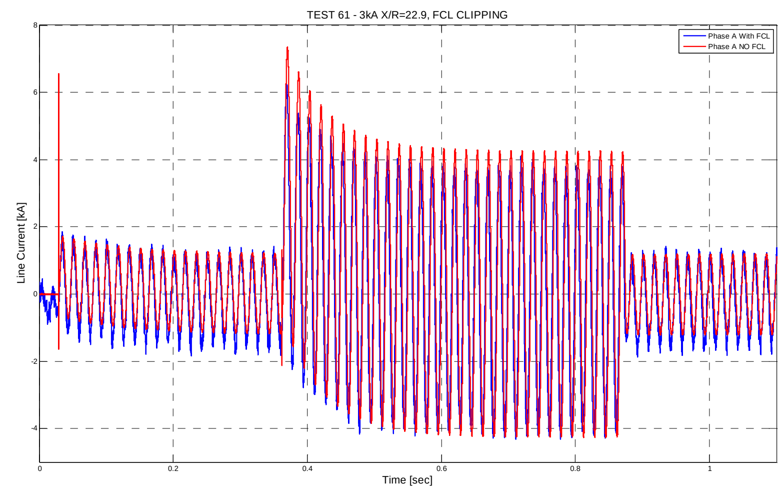


Figure B76: Phase A – 4kA prospective vs. clipped

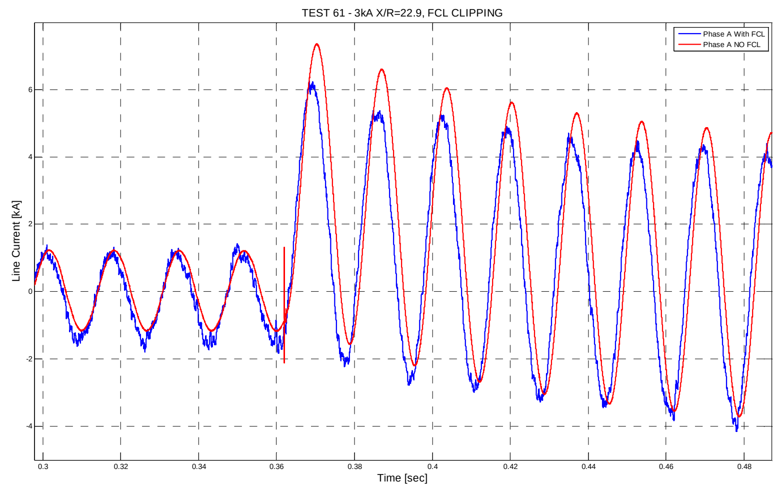


Figure B77: Phase A – 3kA prospective vs. clipped

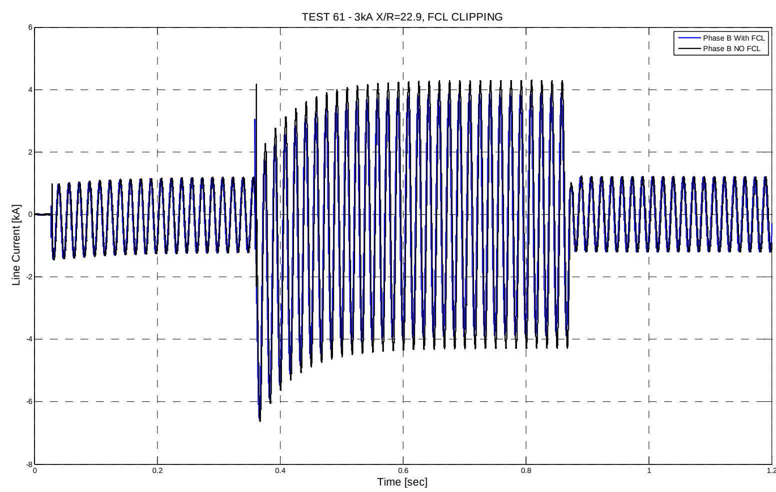


Figure B78: Phase B – 3kA prospective vs. clipped

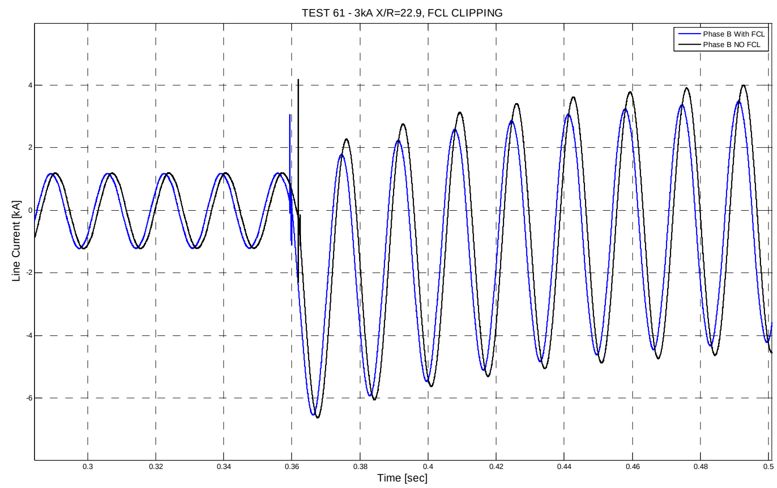


Figure B79: Phase B – 3kA prospective vs. clipped

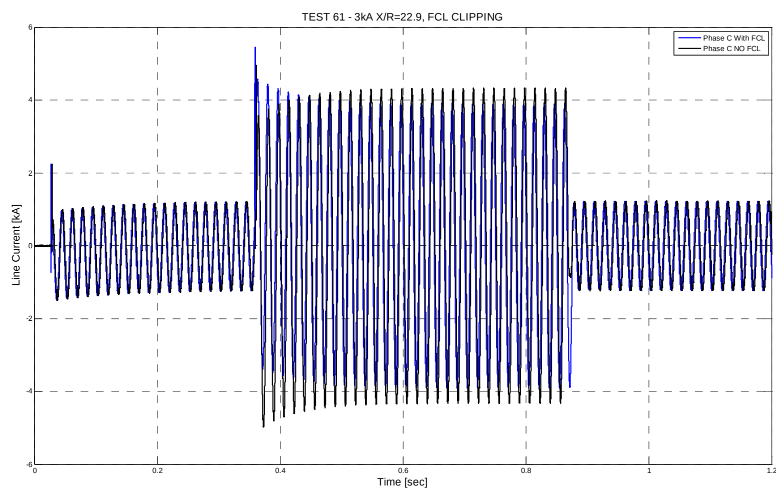


Figure B80: Phase C – 3kA prospective vs. clipped

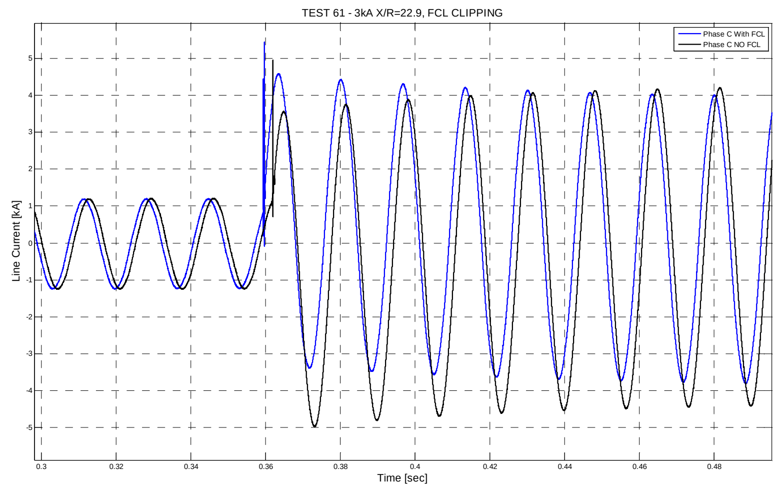


Figure B81: Phase C – 3kA prospective vs. clipped

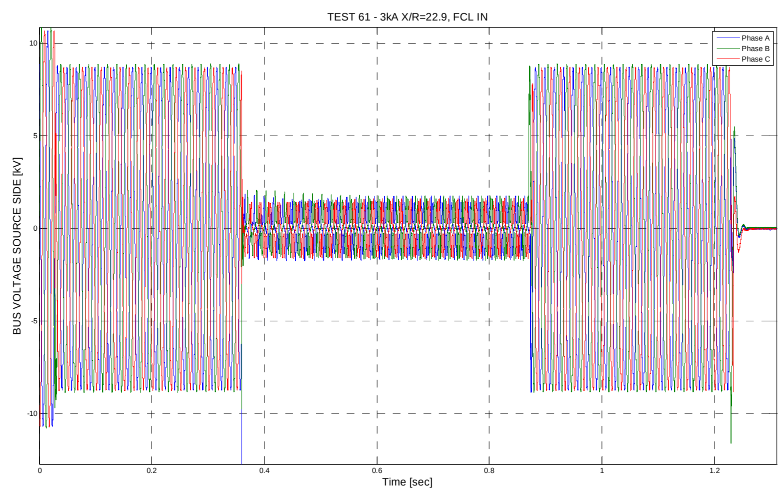


Figure B82: Source Voltage – 3kA

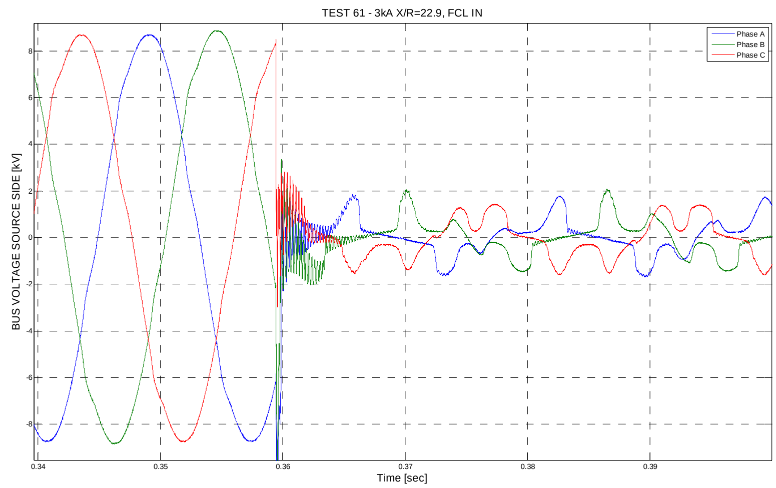


Figure B83: Source Voltage – 3kA - POW

10. APPENDIX C – Additional Fault Tests

10.1 Test 76 - Double Fault Sequence 20kA X/R=21

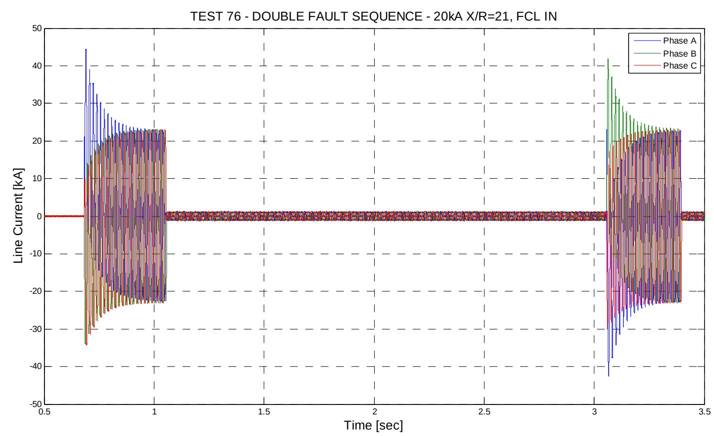


Figure C1: Double fault sequence – 20kA – 2 seconds

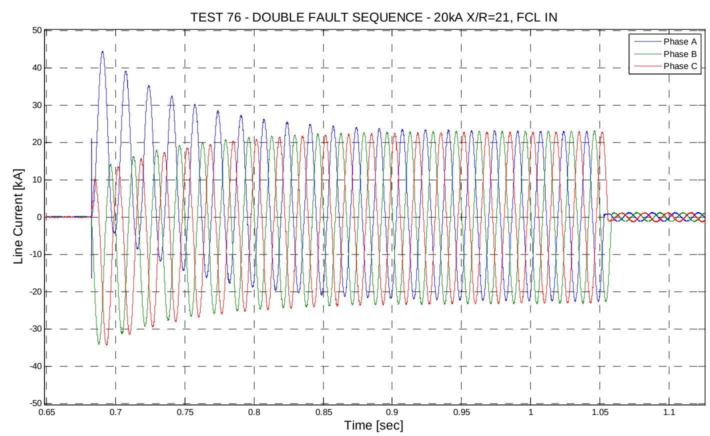


Figure C2: Double fault sequence – 20kA – first 20 cycles

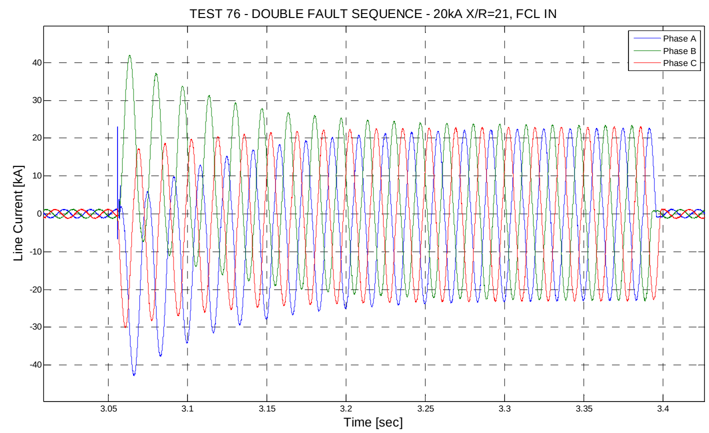


Figure C3: Double fault sequence – 20kA – second 20 cycles

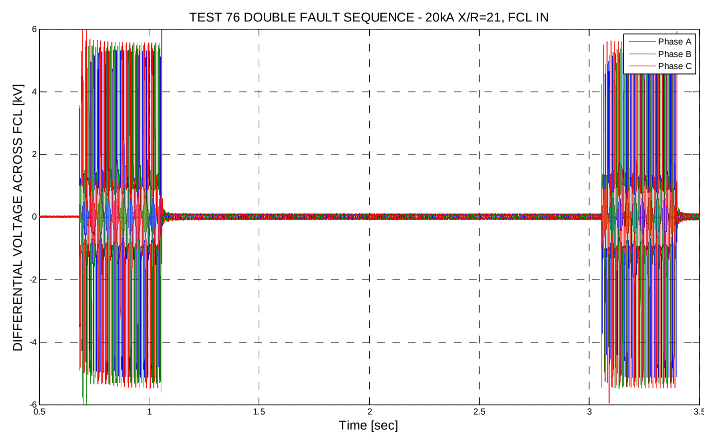


Figure C4: Double fault sequence – 20kA – FCL Voltage

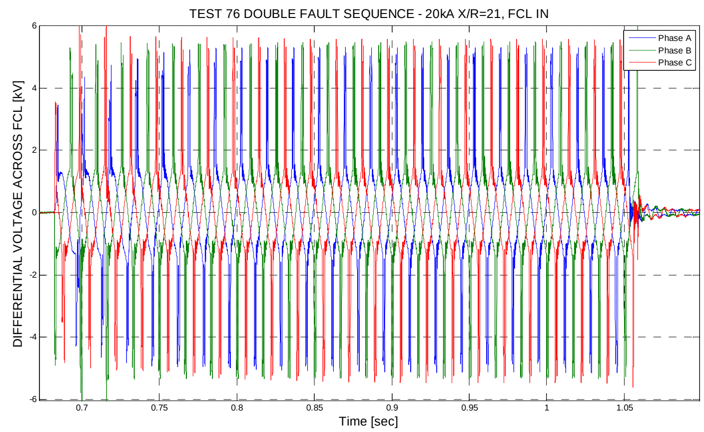


Figure C5: Double fault sequence – FCL Voltage first 20cycles

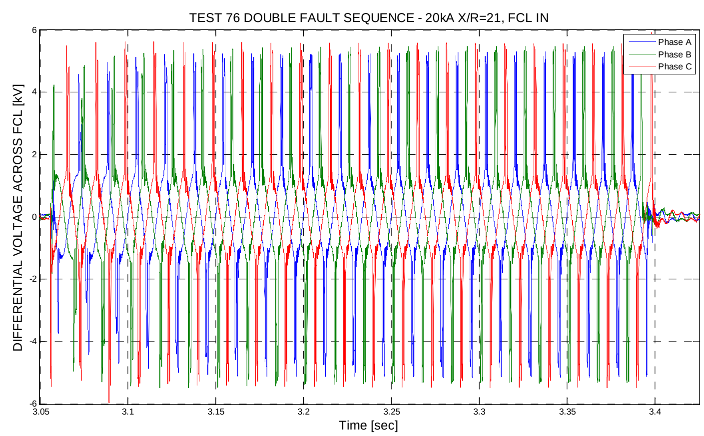


Figure C6: Double fault sequence – FCL Voltage second 20cycles

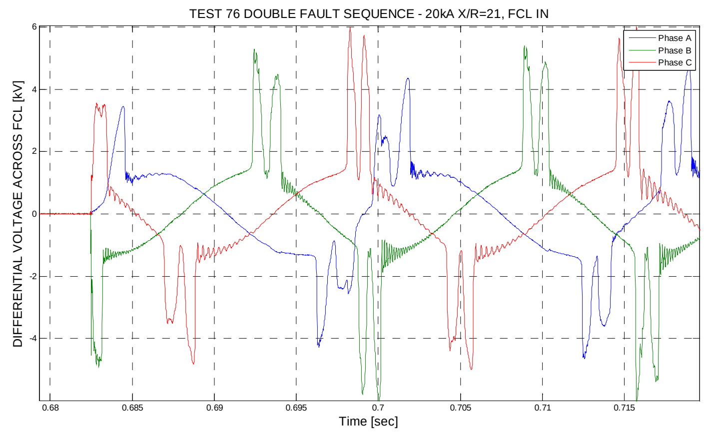


Figure C7: Double fault sequence – FCL Voltage first fault

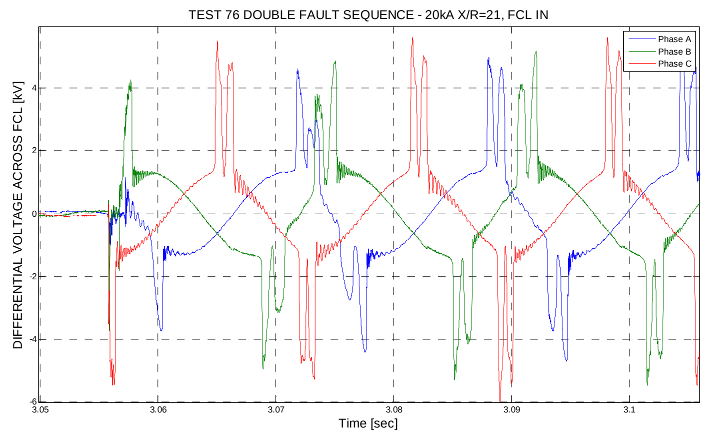


Figure C8: Double fault sequence – FCL Voltage second fault

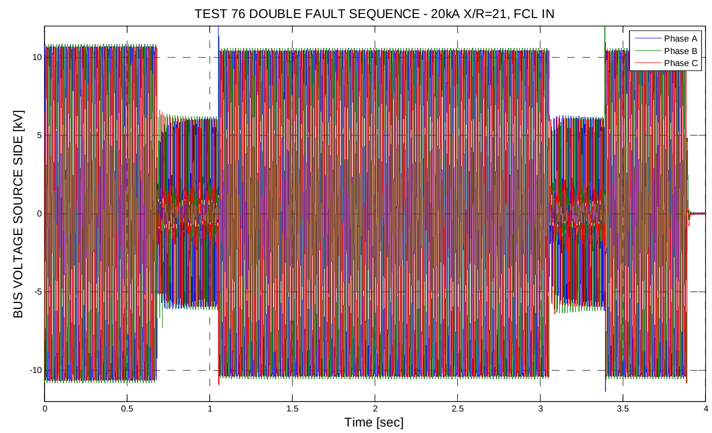


Figure C9: Double fault sequence – Source Voltage

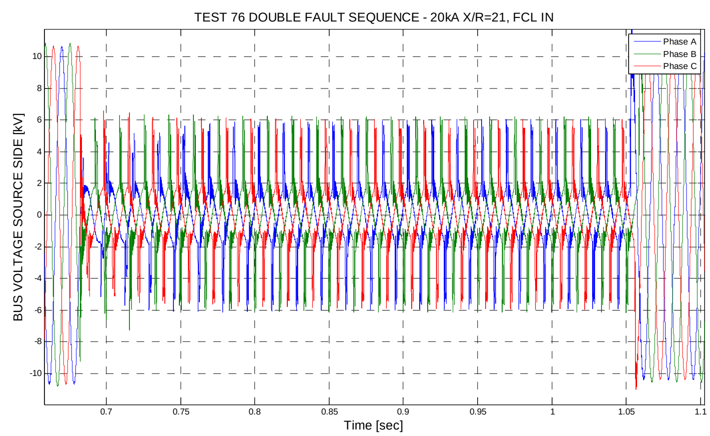


Figure C10: Double fault sequence – Source Voltage first fault

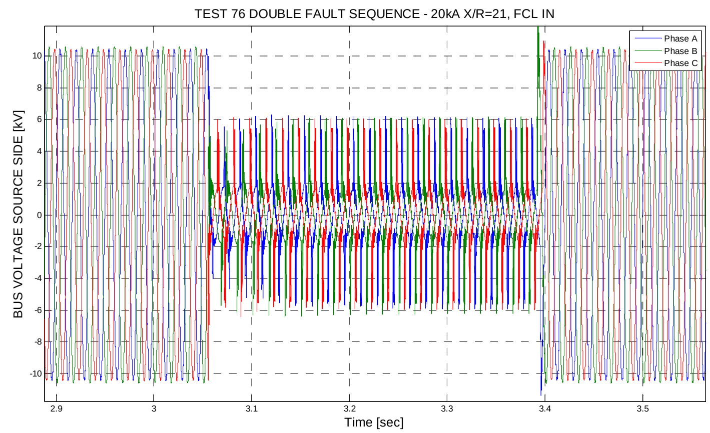


Figure C11: Double fault sequence – Source Voltage second fault

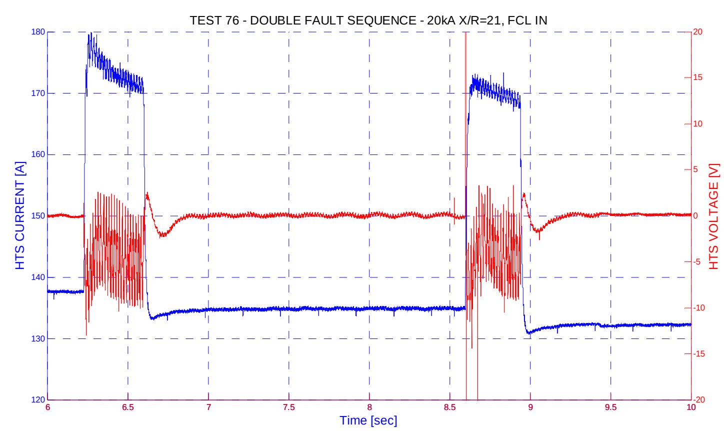


Figure C12: HTS Coil Voltage and Current

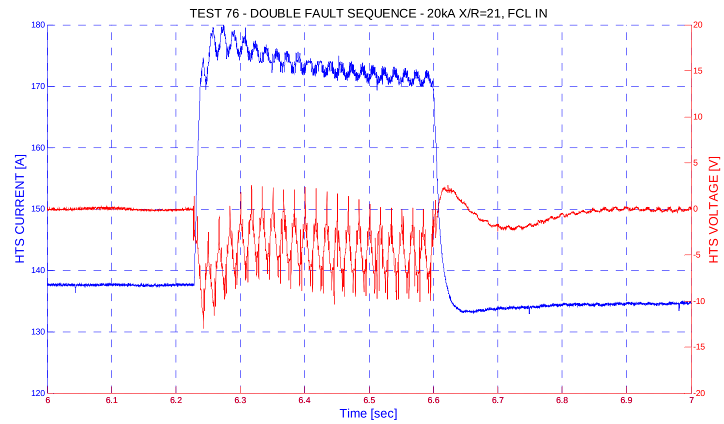


Figure C13: HTS Coil Voltage and Current – first fault

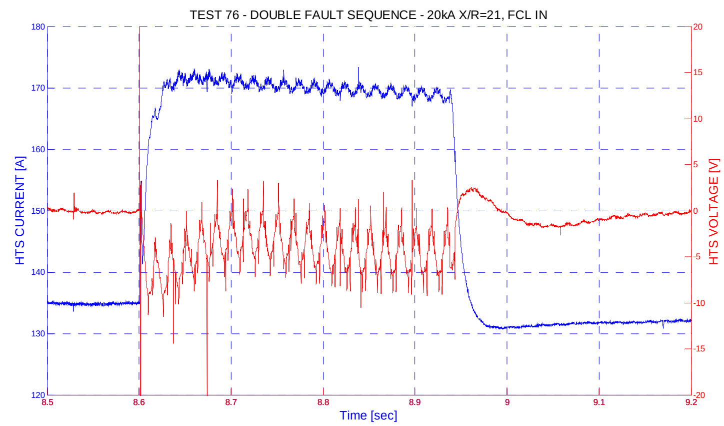


Figure C14: HTS Coil Voltage and Current – second fault

10.2 Test 77 - 1.25s 80-cycle Fault 20kA X/R=21

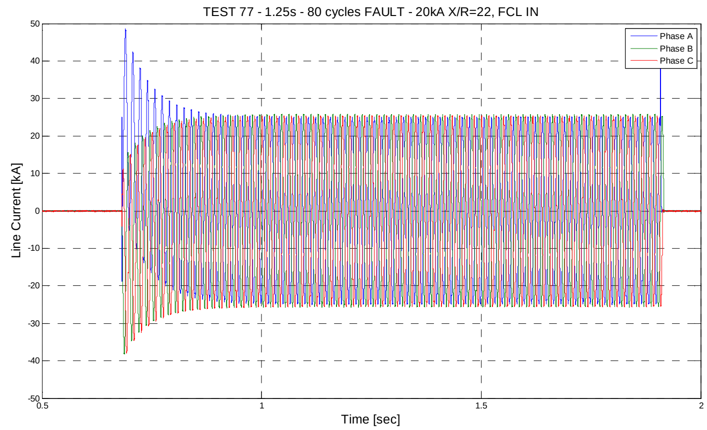


Figure C15: Endurance Test 1.25sec – 20kA

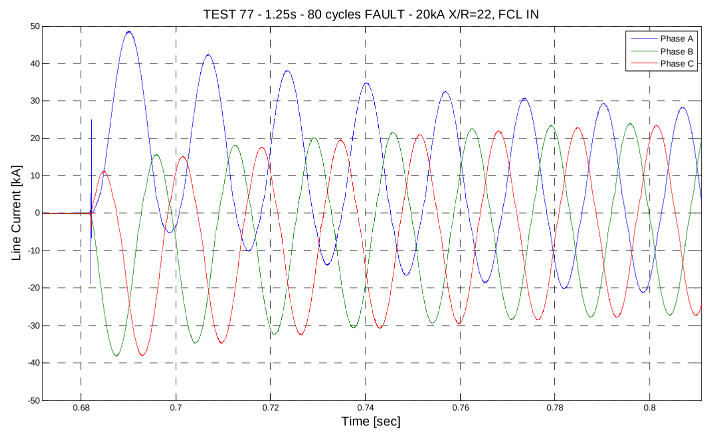


Figure C16: Endurance Test 1.25sec – 20kA

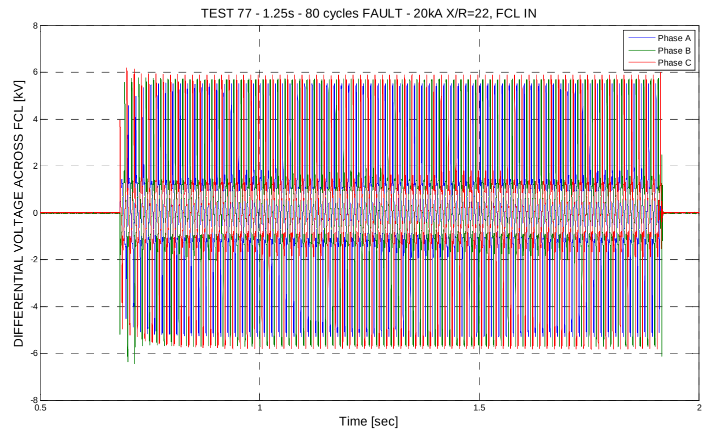


Figure C17: Endurance Test 1.25sec – 20kA – FCL Voltage

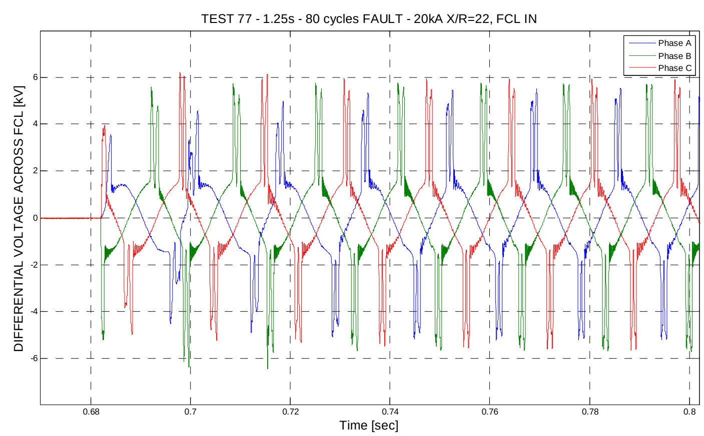


Figure C18: Endurance Test 1.25sec – 20kA – FCL Voltage

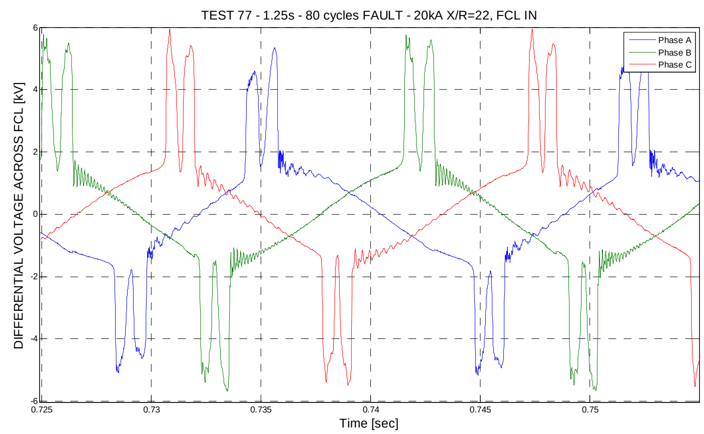


Figure C19: Endurance Test 1.25sec – 20kA – FCL Voltage – zoom

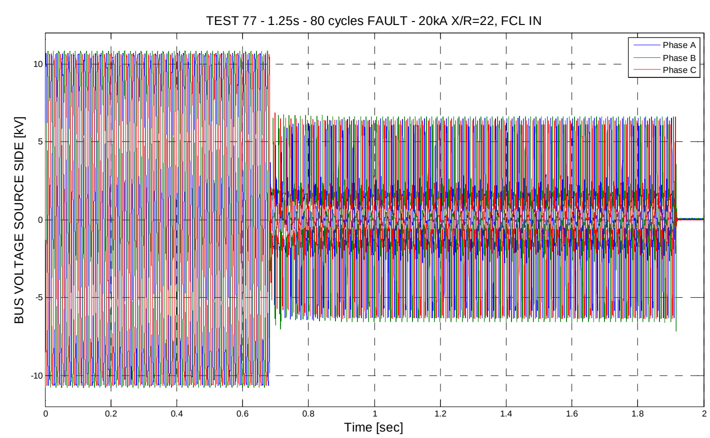


Figure C20: Endurance Test 1.25sec – 20kA – Source Voltage

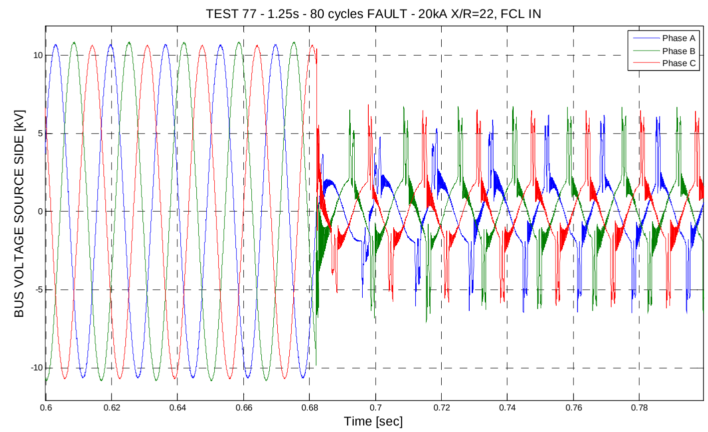


Figure C21: Endurance Test 1.25sec – 20kA – Source Voltage

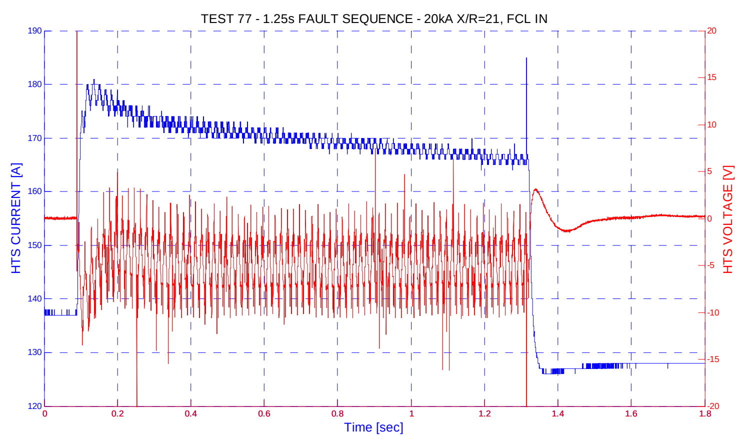


Figure C22: Endurance Test 1.25sec – 20kA – HTS Coil V and I

10.3 Test 78 – Second Double Fault Sequence 20kA X/R=21

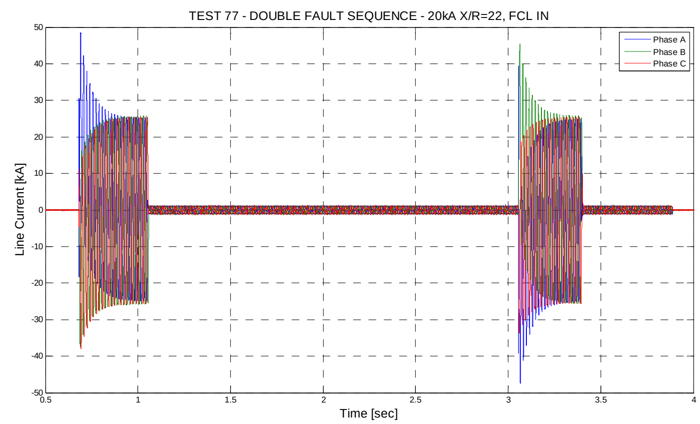


Figure C23: Second Double fault sequence – 20kA – 2 seconds

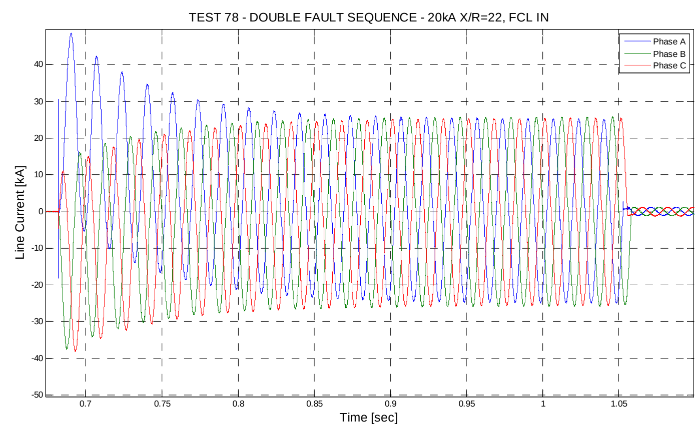


Figure C24: Second Double fault sequence – 20kA – first fault

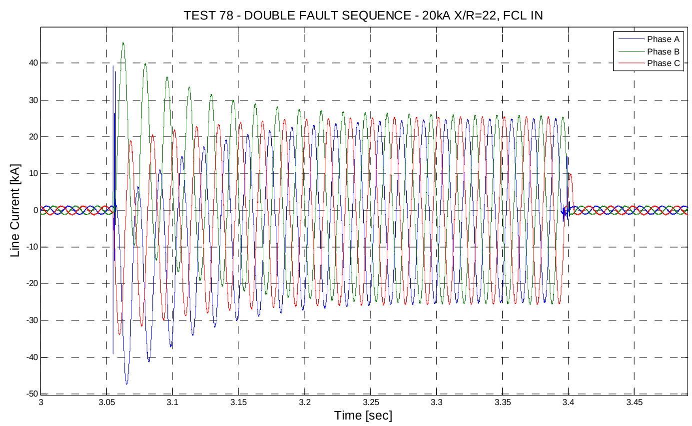


Figure C25: Second Double fault sequence – 20kA – second fault

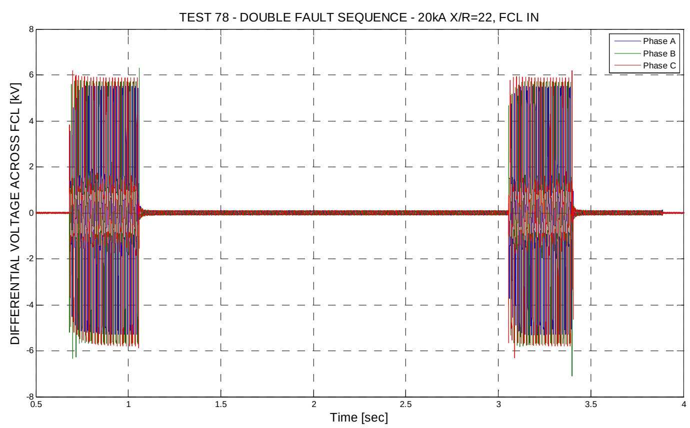


Figure C26: Second Double fault sequence – 20kA – FCL Voltage

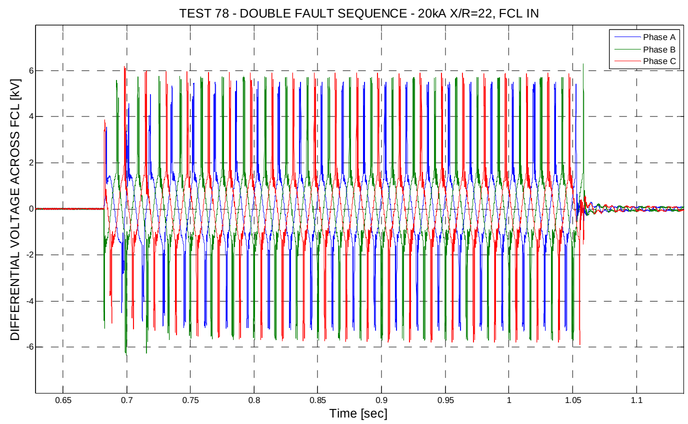


Figure C27: Second Double fault sequence – 20kA – FCL Voltage

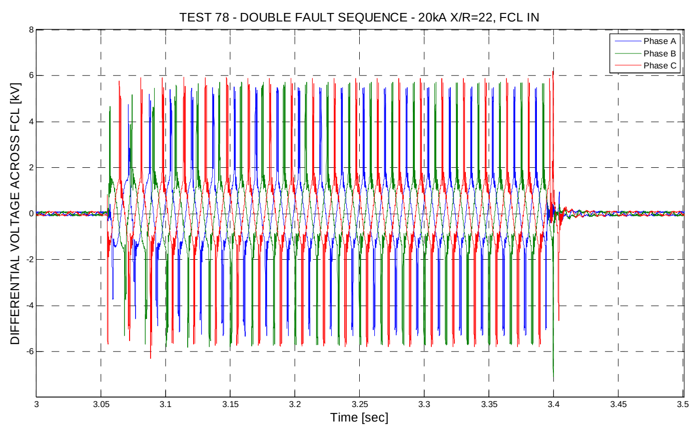


Figure C28: Second Double fault sequence – 20kA – FCL Voltage

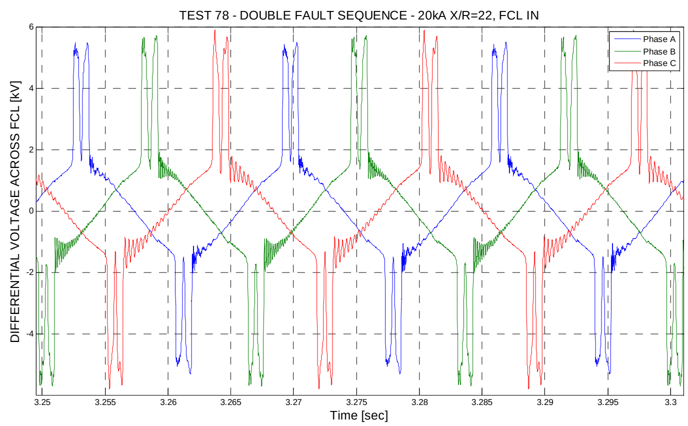


Figure C29: Second Double fault sequence – 20kA – FCL Voltage

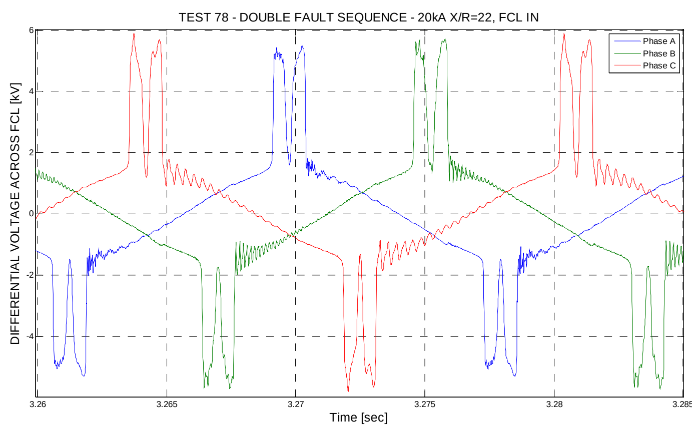


Figure C30: Second Double fault sequence – 20kA – FCL Voltage

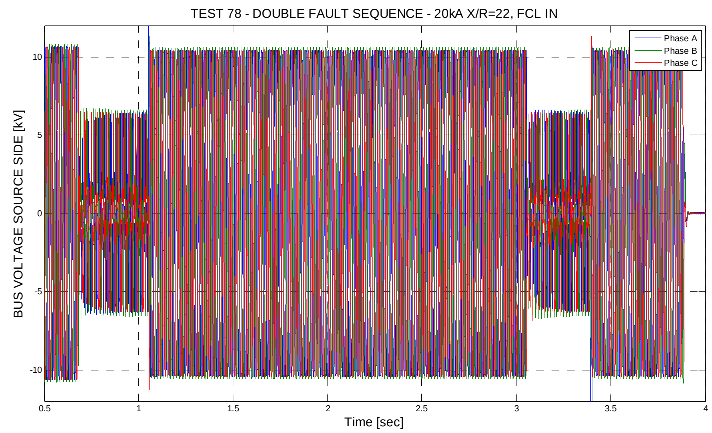


Figure C31: Second Double fault – 20kA – Source Voltage

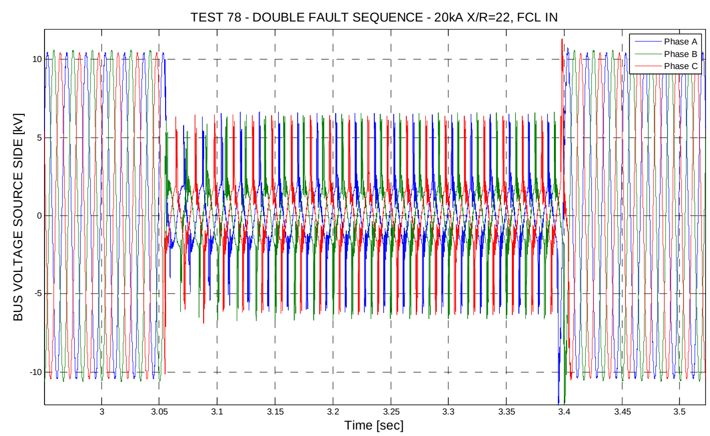


Figure C32: Second Double fault – 20kA – Source Voltage

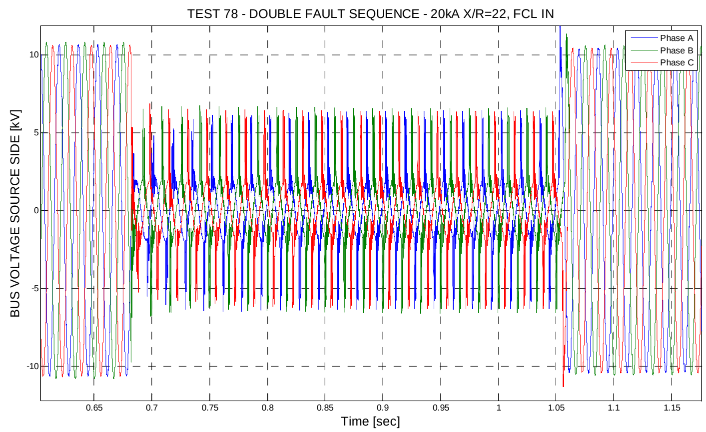


Figure C33: Second Double fault – 20kA – Source Voltage

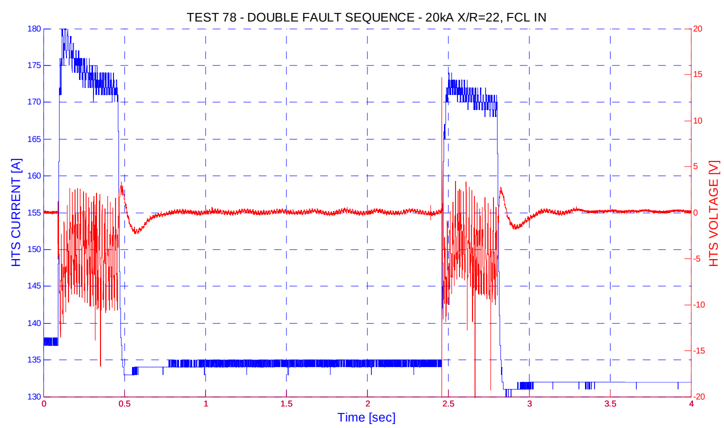


Figure C34: Second Double fault – 20kA – HTS Coil V and I

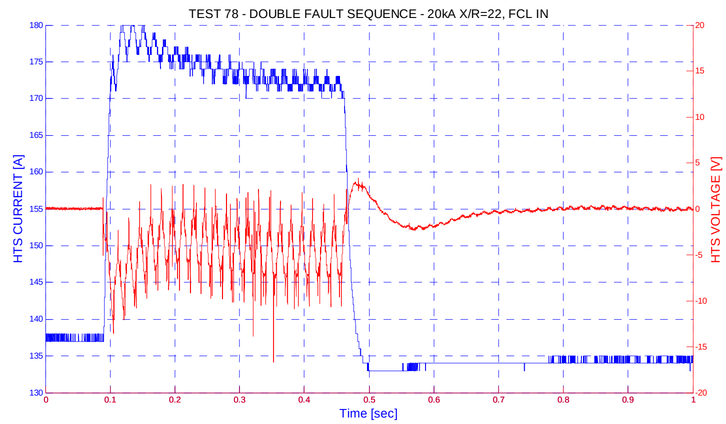


Figure C35: Second Double fault – 20kA – HTS Coil V and I

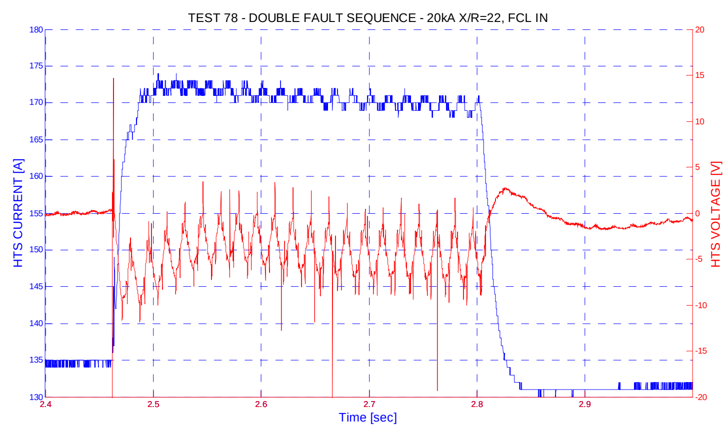


Figure C36: Second Double fault – 20kA – HTS Coil V and I

11. APPENDIX D – Powertech Source and Load Impedances

No.	Reactance @60 Hz at phase			Maximum Current		One shot I2t @30C	X/R at 20C	Continuous current
#	A	B	C	kArms	kApeak	A2s	-	Arms
1	0.0021	0.0022	0.0021	84.7	244	3.8E+11	95	4000
2	0.0044	0.0042	0.0040	84.9	237	1.8E+11	90	4000
3	0.0083	0.0082	0.0082	80.2	224	1.2E+11	89	4000
4	0.0165	0.0166	0.0165	72.2	201	5.0E+10	84	3000
5	0.0320	0.0339	0.0325	60.2	168	2.2E+10	69	2700
6	0.0630	0.0671	0.0609	45.2	126	1.1E+10	79	1900
7	0.1316	0.1292	0.1315	32.0	89	5.8E+09	75	1900
8	0.2590	0.2640	0.2590	23.0	64	4.2E+09	89	1100
9	0.5300	0.5180	0.5210	16.4	46	1.8E+09	94	750
10	1.0400	1.0290	1.0360	11.6	32	7.6E+08	79	450
11	2.1000	2.0700	2.1000	7.5	21	4.8E+08	82	300
12	4.2200	4.2100	4.2300	4.5	12	2.0E+08	82	220
13	8.3900	8.3100	8.3100	2.5	7	1.2E+08	83	160
14	16.9200	17.0900	16.9600	1.3	4	5.8E+07	83	110
15	33.6900	34.3500	34.1000	0.7	2	3.0E+07	77	80
Sum 1-13	16.80	16.66	16.71	-	-	-	-	

Table D1: Source Reactance Values

	mOhms	kA	MJ
R1	4.5	20	16
R2	8.5	20	32
R3	18.1	20	64
R4	31.3	20	72
R5	70.2	20	144
R6	122	20	128
R7	269	18.3	144
R8	488	9.3	128
R19	888	4.6	144
R10	2132	2.3	128
R11	4247	1.2	64

Table D2: Source Resistor Values

Name	A phase Ohms	B phase Ohms	C phase Ohms	Energy J	Imax Arms	Icont Arms
LR1	2.06	2.08	2.08	6.0E+06	750	105
LR2	4.16	4.16	4.19	1.2E+07	750	105
LR3	8.27	8.35	8.38	2.4E+07	750	105
LR4	16.80	16.92	16.77	4.8E+07	750	105
LR5	29.50	29.70	29.60	6.0E+07	600	85
LR6	63.00	63.10	63.20	3.0E+07	300	50

Table D3: Load Resistor Values

List of Revisions

Revision	Date	Action	Modified Page
1	11/07/08	First Released	

APPENDIX F:
Zenergy Power HTS FCL High Voltage Field Test

Test Report

Reporting Center (full name and address):			Zenergy Power Inc. 379 Oyster Point Blvd., Suite 1 South San Francisco, CA USA 94080-1961 Tel.: +1-650-615-5700		
Responsible Person:	Francisco De La Rosa				
Project Name:	CEC Avanti				
Document Title:	High Voltage Testing SCE SSID-ESI				
Document Ref.No.:	**ZP/TR-2008/04**	Reg: #		Page 1	
Date of issue:	12/17/08	Classification:	Confidential	No. of pages:	44
Client(s):	CEC/SCE				
Author(s):	F. De La Rosa F. Moriconi W. Schram A. Singh	Approved:	F. Moriconi	Order No.:	
Distribution:	A. Kamiab (SCE), Alan Hood (SCE), K. Smedley (CEC UC Irvine), F. Moriconi, W. Schram, R. Lombaerde, A. Singh, M. Levitskaya, F. De La Rosa, A. Singh (ZP USA)				
Distribution page 1:	B. Nelson, W. Gibson, A. Rodriguez, S. Ramsay (ZP USA), F. Darmann (ZP AUS), C. Buehrer (ZP DE)				
Keywords:	Fault Current Limiter, High Voltage tests, Lightning impulse test, full wave, chopped wave, BIL, Avanti Circuit				

Summary:
This report presents the results of the additional high voltage tests conducted to the CEC Avanti FCL at SCE SSID-ESI facilities in Westminster, CA. Testing included a 5 kV DC insulation test followed by reduced and full lightning and chopped waves per IEEE C57.12.01-2005 and ending with a 15 kV applied voltage test.

Contents **Page**

1. Applicability

Saturable-core HTS Fault Current Limiter 15kV class, 750A.

2. Documentation

[1] Test Plan for Additional FCL Testing, ZP/ER_2008/06 Rev 1, ZP Internal Report

[2] NETA-Acceptance Testing Specifications for Electrical Power Distribution Equipment and Systems, 2007

3. Acronyms and definitions

3.1 Acronyms

FCL	Fault Current Limiter
HTS	High Temperature Superconductor
CEC	California Energy Commission
SCE	Southern California Edison

3.2 Definitions

Ambient temperature: this is the temperature of the air surrounding the FCL. For the purposes of IEEE Std C57.16-1996, it is assumed that the temperature of the cooling air (ambient temperature) does not exceed 40 ^{o} C and the average temperature of the cooling air for any 24 hour period does not exceed 30 ^{o} C.

4. General

The results from the additional high voltage and insulation tests conducted to the CEC Avanti FCL are described in this report. HV tests were successful and FCL insulation and AC voltage withstand after impulse voltage tests was preserved. All tests were based on the test plan described in [1].

5. Insulation tests

5.1 FCL AC terminals

Insulation of the FCL was tested as part of a routine check SSID-ESI carries out prior to subjecting an object to BIL testing. A 1000 VDC insulation resistance (megger) test was applied between every phase on the source side and ground during one minute and the resultant insulation resistance from the instrument display was read. The results obtained are described in table 1. All of them are above the minimum 5000MΩ recommended by NETA [2] for equipment with operating voltages up to 15 kV.

A Phase to Ground Insulation Resistance GΩ	B Phase to Ground Insulation Resistance GΩ	C Phase to Ground Insulation Resistance GΩ
156	151	206

Table 1. Insulation resistance test on the FCL

5.2 Potential Transformers (PT's)

Insulation resistance was also practiced on the PT's located in the small enclosure on the load side of the FCL. The insulation of these PT's had not been tested previously. Tests were conducted on the primary and secondary of the PT's and yielded results as per table 2. The obtained insulation levels are extraordinarily high, well above the 5000 MΩ desired level [2].

PT's Primary Side			PT's Secondary Side		
A Phase to Ground Insulation Resistance GΩ	B Phase to Ground Insulation Resistance GΩ	C Phase to Ground Insulation Resistance GΩ	A Phase to Ground Insulation Resistance GΩ	B Phase to Ground Insulation Resistance GΩ	C Phase to Ground Insulation Resistance GΩ
426	595	550	376	408	496

Table 2. FCL PT's insulation resistance test

6. Lightning impulse tests

These tests consisted on the application of chopped wave impulse tests on every phase of the FCL between a common point connecting source and load ends and ground. The tests comprised:

a. One reduced (1.2 x 50 μs) full wave– 50% or 55 kV peak wave
b. One full (1.2 x 50 μs) wave – 100% or 110 kV peak wave
c. One reduced chopped wave – 50% or 60 kV peak wave
d. Two full chopped waves - 100% or 120 kV peak waves
e. Two full (1.2 x 50 μs) waves (preferably within 10 min after the last chopped wave)

With chopped wave crest voltage and time to chop as indicated in table 1.

Nominal system voltage (kV)	BIL and full wave (kV) crest	Chopped-Wave (kV) crest	Time to flashover (μs)
15.0	110	120	2.0

Table 3: Lightning Impulse Voltage amplitude and time to chop used in the tests, per EEE Std C57.16-1996 [1]

The tests were conducted with no DC bias current on the HTS coil.

7. Impulse voltage test results

Test results assembled and documented by SSID are presented in Appendix A. It is noteworthy to notice that after all insulation enhancements performed on the FCL, it successfully passed the lightning impulse tests required in the test plan.

8. Conclusions

The tests conducted at SCE SSID high voltage laboratory on the CEC Avanti FCL are described in this report. The FCL endured well and passed the applied tests.

List of Tables and Figures

List of Revisions

Revision	Date	Action	Modified Page
1	12/17/08	Released	

9. APPENDIX 1

SSID REPORT ON HIGH VOLTAGE TESTS TO THE CEC AVANTI FCL

12.12.2008

T E S T   R E P O R T

Company Name	Zenergy
Serial Number	~~T08-32-2188~~ N08JH50227
Customer Name	Zenergy
Order Number	
Comment	

Manufacturer	Zenergy	Air Temp.
Test Object	CLR	Air Pressure
	New test for Qualifica	Air Humidity

Test Leader	Larry Baisden
Test Engineer	Ray Antonio
Inspector	
Standard	

Directory C:\DATA\

ARFW2.DAT 12 FW 50%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 110kV	55kV 15.54%		1.25us	38.9us				
B,C 151.5 V/V Full Ampl. 110kV	55.6kV		1.19us					

AFW1.DAT 13 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 110kV	110kV 15.71%		1.26us	39.1us				
B,C 151.5 V/V Full Ampl. 110kV	111kV		1.2us					

ARCW.DAT 15 CW 50%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 121kV	60.1kV	-24.04%	1.25us		2.44us			
B,C 151.5 V/V Full Ampl. 121kV	60.6kV	-29.54%	1.18us		2.55us			

Directory C:\DATA\

ACW1.DAT 16 CW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 121kV	118kV	-32.78%	1.23us		1.47us			
B,C 151.5 V/V Full Ampl. 121kV	121kV	-34.71%	1.19us		1.55us			

ACW2.DAT 17 CW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 121kV	119kV	-23.48%	1.25us		2.25us			
B,C 151.5 V/V Full Ampl. 121kV	121kV	-28.93%	1.2us		2.35us			

AFW2.DAT 18 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 110kV	110kV 15.56%		1.26us	38.9us				
B,C 151.5 V/V Full Ampl. 110kV	111kV		1.2us					

AFW3.DAT 19 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
A 151.5 V/V Full Ampl. 110kV	110kV 15.56%		1.26us	38.8us				
B,C 151.5 V/V Full Ampl. 110kV	111kV		1.2us					

BRFW.DAT 20 FW 50%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 110kV	55.1kV 15.77%		1.23us	38.7us				
B 151.5 V/V Full Ampl. 110kV	55.7kV		1.17us					

Directory C:\DATA\

BFW1.DAT 21 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 110kV	110kV 15.55%		1.23us	39us				
B 151.5 V/V Full Ampl. 110kV	111kV		1.17us					

BRCW.DAT 22 CW 50%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 121kV	60.2kV	-23.16%	1.22us		2.45us			
B 151.5 V/V Full Ampl. 121kV	60.7kV	-28.82%	1.16us		2.55us			

BCW1.DAT 23 CW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 121kV	120kV	-23.3%	1.23us		2.34us			
B 151.5 V/V Full Ampl. 121kV	121kV	-28.69%	1.17us		2.44us			

BCW2.DAT 24 CW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 121kV	120kV	-23.55%	1.23us		2.34us			
B 151.5 V/V Full Ampl. 121kV	121kV	-28.66%	1.18us		2.46us			

BFW2.DAT 25 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 110kV	110kV 15.53%		1.23us	39us				
B 151.5 V/V Full Ampl. 110kV	111kV		1.18us					

Directory C:\DATA\

BFW3.DAT 26 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
B 151.5 V/V Full Ampl. 110kV	110kV 15.66%		1.24us	39.1us				
B 151.5 V/V Full Ampl. 110kV	111kV		1.18us					

CRFW.DAT 27 FW 50%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 110kV	55.2kV 15.89%		1.24us	38.8us				
C 151.5 V/V Full Ampl. 110kV	55.8kV		1.18us					

CFW1.DAT 28 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 110kV	110kV 16.06%		1.24us	38.8us				
C 151.5 V/V Full Ampl. 110kV	112kV		1.19us					

CRCW.DAT 29 CW 50%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 121kV	60.3kV	-23.71%	1.24us		2.41us			
C 151.5 V/V Full Ampl. 121kV	60.8kV	-29.52%	1.18us		2.5us			

CCW1.DAT 30 CW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 121kV	120kV	-23.81%	1.24us		2.32us			
C 151.5 V/V Full Ampl. 121kV	121kV	-29.2%	1.18us		2.45us			

Directory C:\DATA\

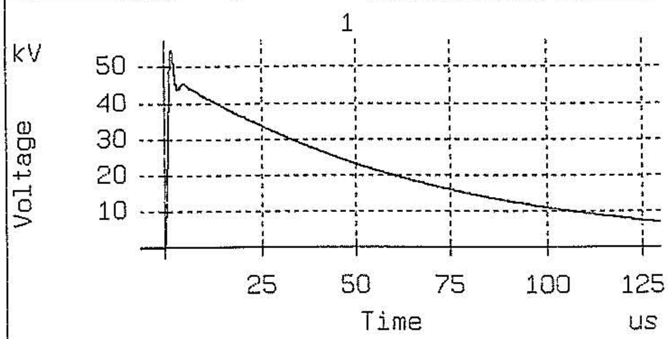
CCW2.DAT 31 CW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 121kV	120kV	 -28.95%	1.24us		1.68us			
C 151.5 V/V Full Ampl. 121kV	121kV	 -34.49%	1.18us		1.76us			

CFW2.DAT 32 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 110kV	110kV 15.91%		1.25us	38.6us				
C 151.5 V/V Full Ampl. 110kV	112kV		1.19us					

CFW3.DAT 33 FW 100%	Max Over	Min Under	T1	T2	Tc	Tp	Td	T0
C 151.5 V/V Full Ampl. 110kV	110kV 15.93%		1.25us	38.8us				
C 151.5 V/V Full Ampl. 110kV	112kV		1.19us					

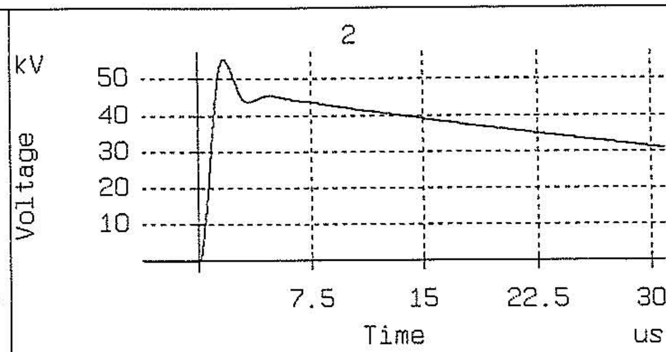
The test object has passed the specified test.

Sign(s) :



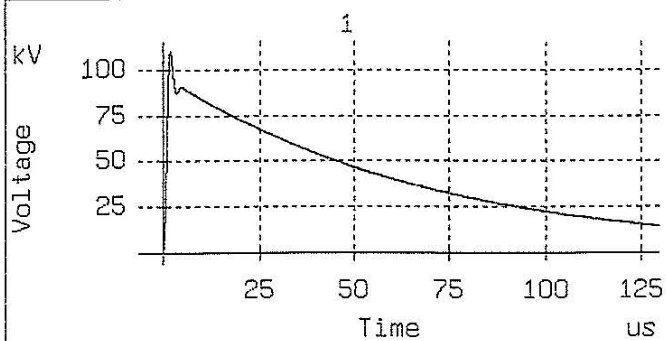
A 50% LI full

55kV T1=1.25us T2=38.9us



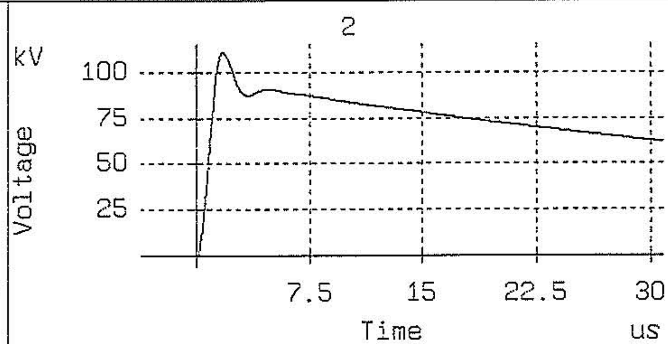
B,C 50% LI full

55.61kV T1=1.19us T2=--



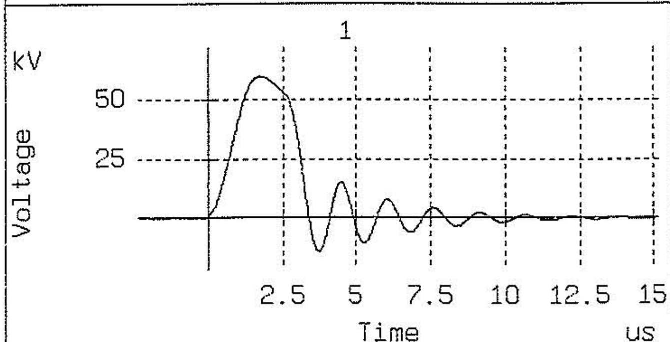
A 100% LI full

109.8kV T1=1.26us T2=39.1us



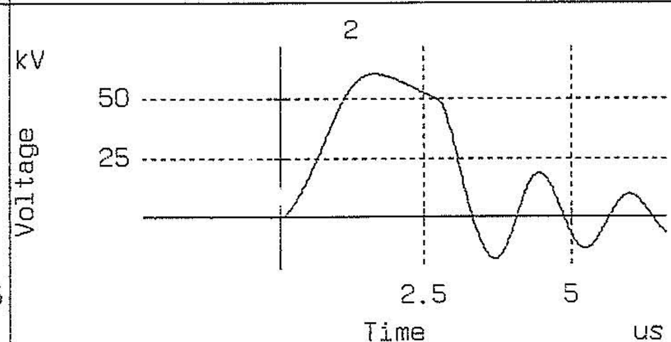
B,C 100% LI full

111.1kV T1=1.2us T2=--



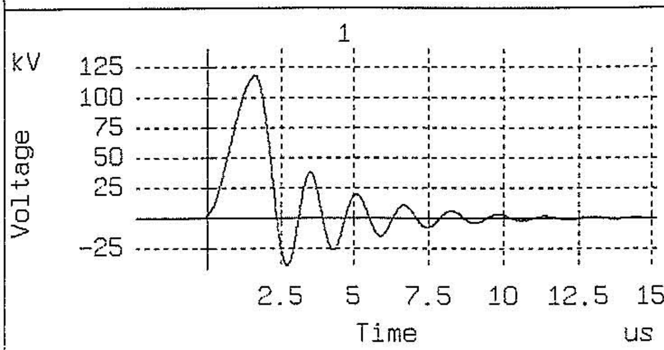
A 50% LI tail chopped

60.06kV -24.04% T1=1.25us Tc=2.44us



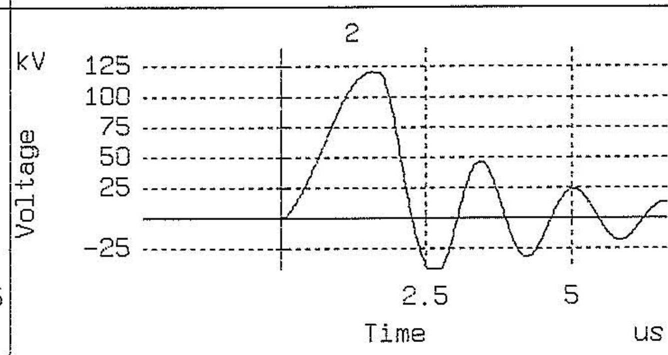
B,C 50% LI tail chopped

60.55kV -29.54% T1=1.18us Tc=2.55us



A 100% LI tail chopped

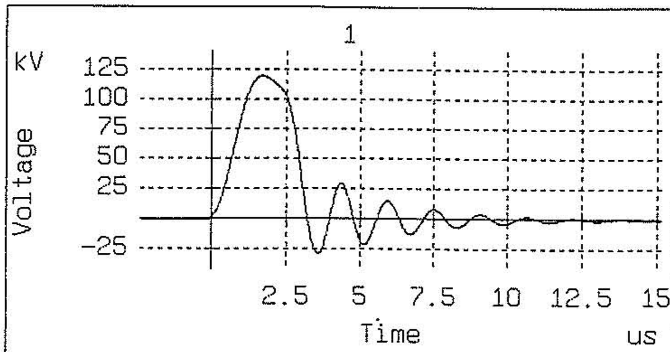
118.3kV -32.78% T1=1.23us Tc=1.47us



B,C 100% LI tail chopped

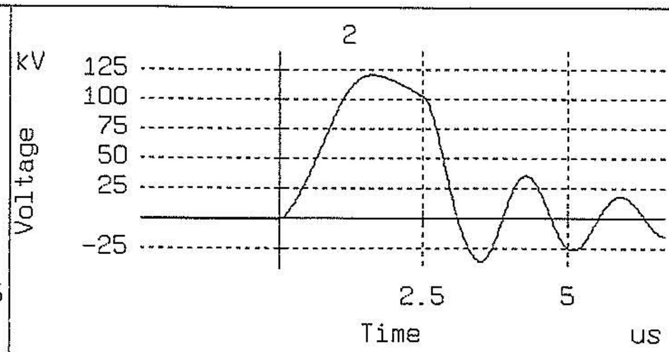
120.6kV -34.71% T1=1.19us Tc=1.55us U

12.12.2008



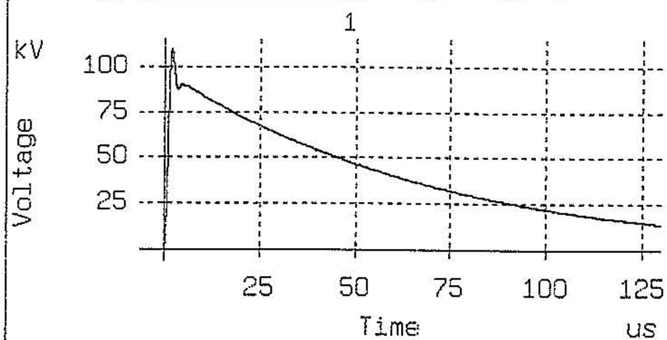
A 100% LI tail chopped

119.5kV -23.48% T1=1.25us Tc=2.25us



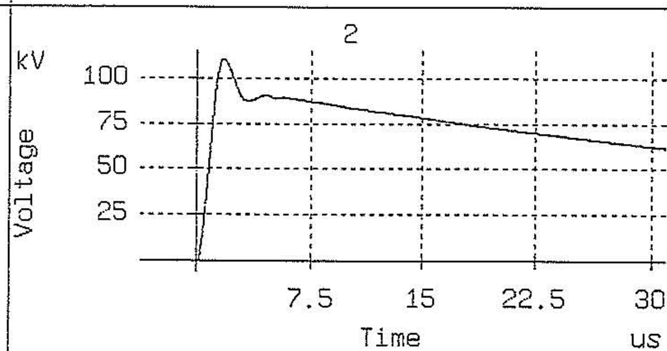
B,C 100% LI tail chopped

120.6kV -28.93% T1=1.2us Tc=2.35us



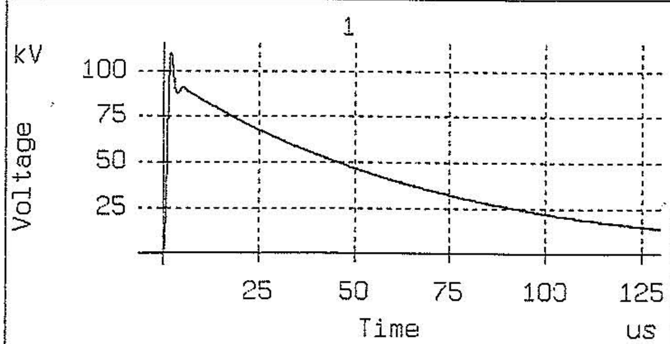
A 100% LI full

109.7kV T1=1.26us T2=38.9us



B,C 100% LI full

111.1kV T1=1.2us T2=--



A 100% LI full

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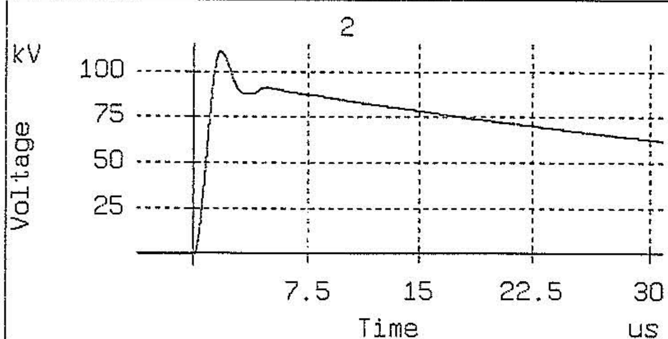
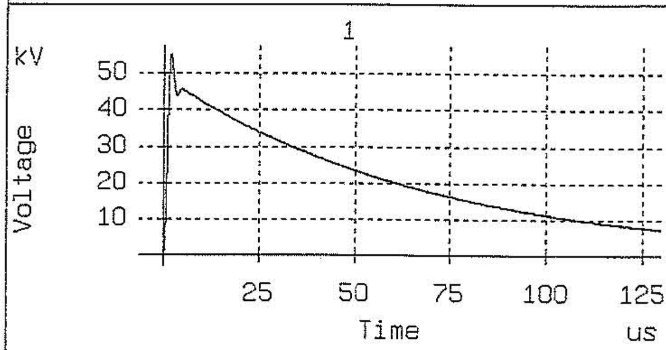


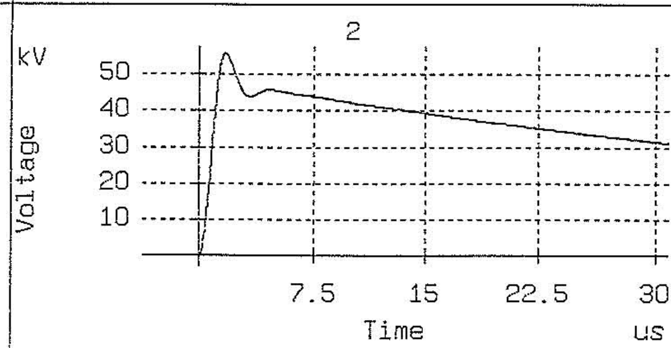
B,C 100% LI full

111.1kV T1=1.2us T2=--



B 50% LI full

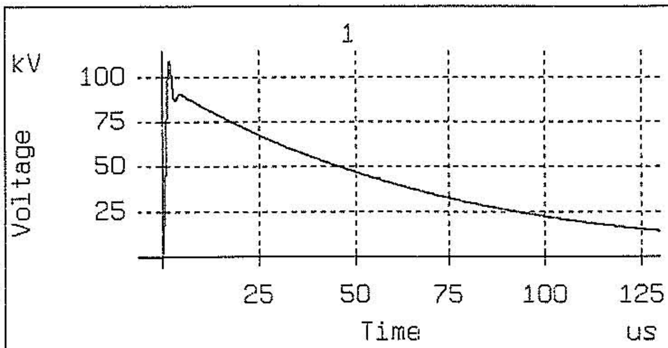
55.11kV T1=1.23us T2=38.7us



B 50% LI full

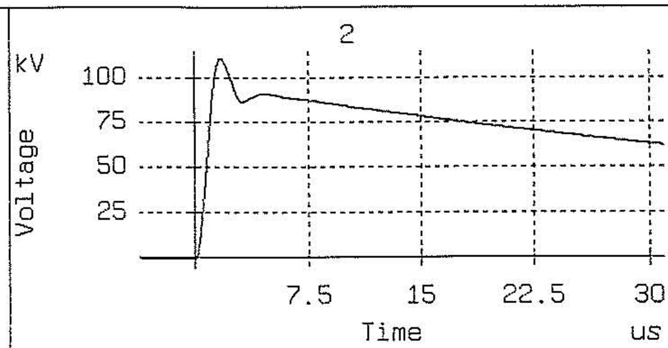
55.72kV T1=1.17us T2=--

12.12.2008



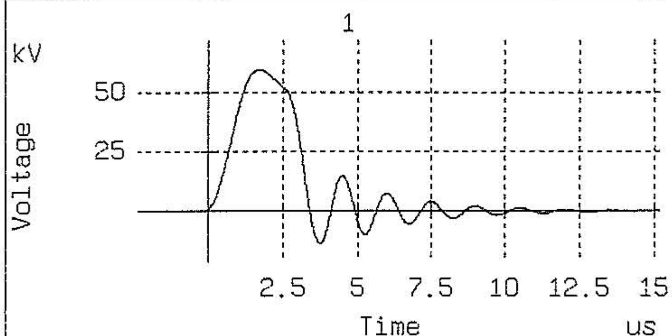
B 100% LI full

110kV T1=1.23us T2=39us



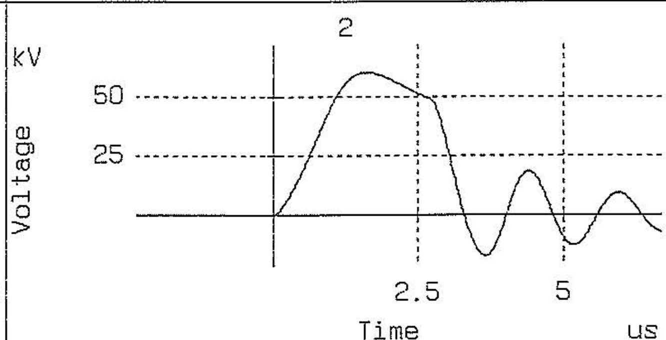
B 100% LI full

111.2kV T1=1.17us T2=--



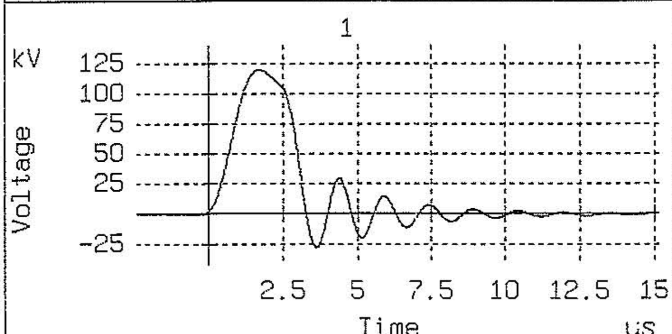
B 50% LI tail chopped

60.19kV -23.16% T1=1.22us Tc=2.45us



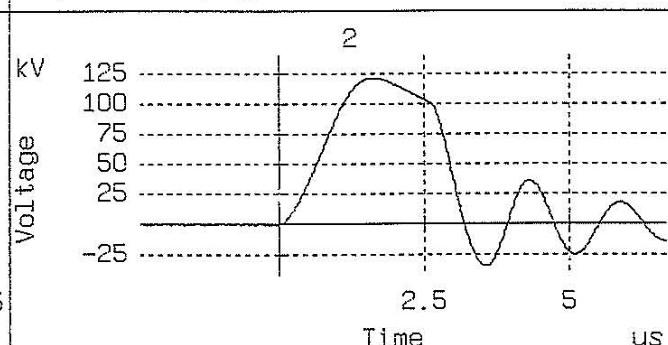
B 50% LI tail chopped

60.75kV -28.82% T1=1.16us Tc=2.55us



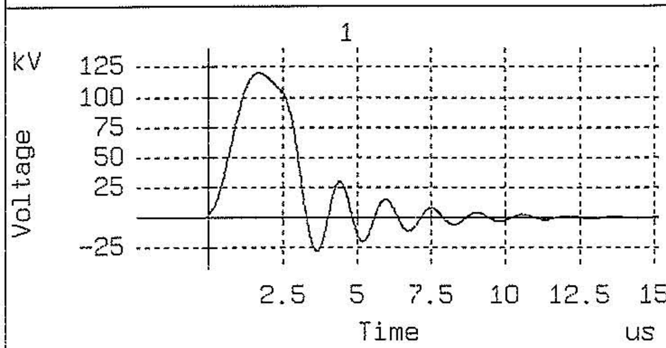
B 100% LI tail chopped

119.9kV -23.3% T1=1.23us Tc=2.34us



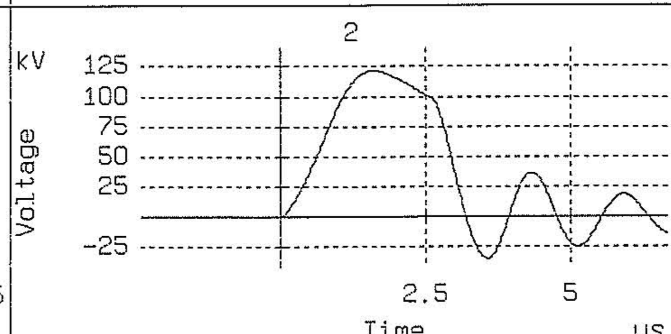
B 100% LI tail chopped

121kV -28.69% T1=1.17us Tc=2.44us



B 100% LI tail chopped

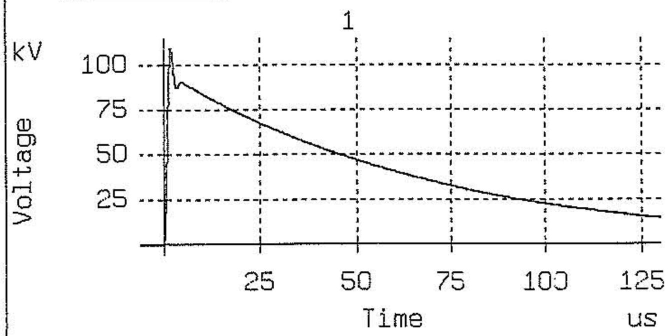
119.8kV -23.55% T1=1.23us Tc=2.34us



B 100% LI tail chopped

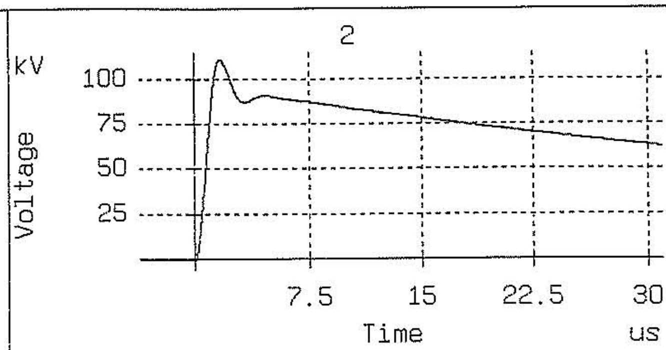
121.2kV -28.66% T1=1.18us Tc=2.46us

12.12.2008



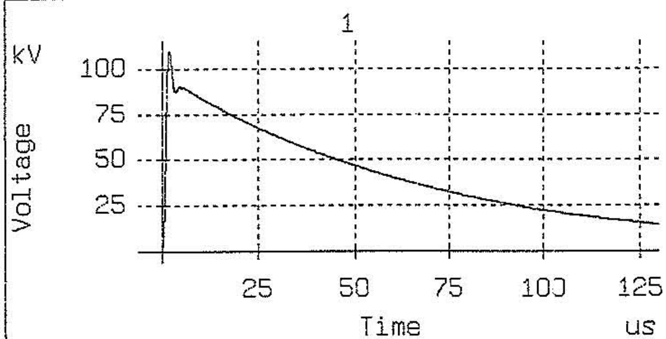
B 100% LI full

110.1kV T1=1.23us T2=39us



B 100% LI full

111.2kV T1=1.18us T2=--



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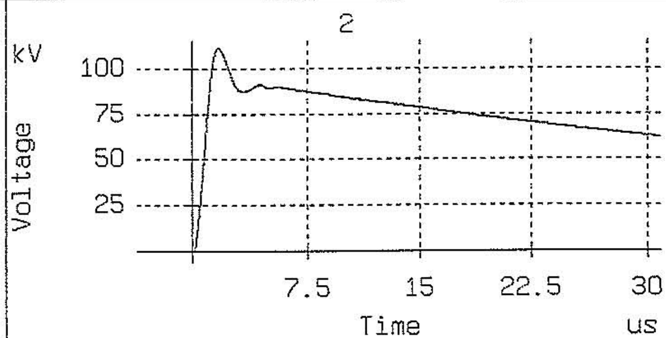
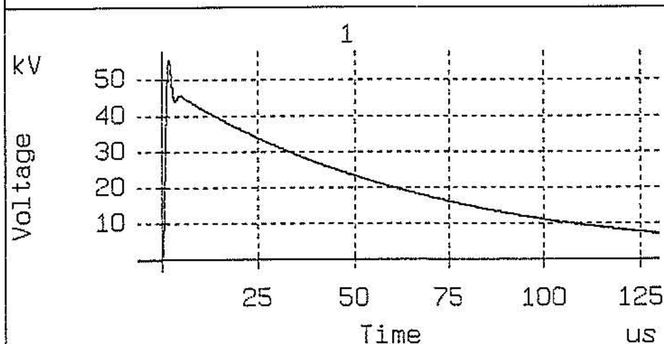


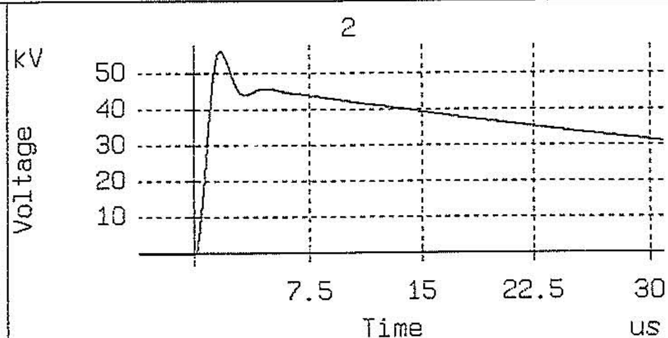
B 100% LI full

111.3kV T1=1.18us T2=--



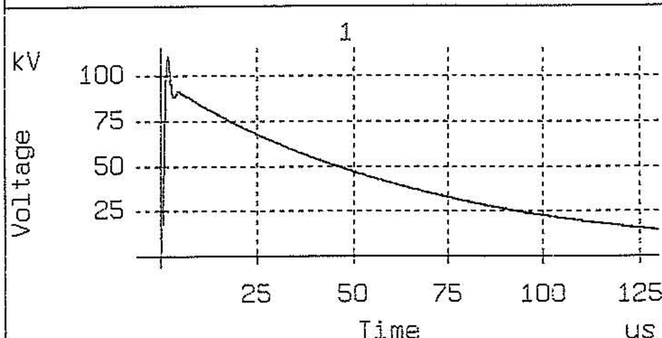
C 50% LI full

55.18kV T1=1.24us T2=38.8us



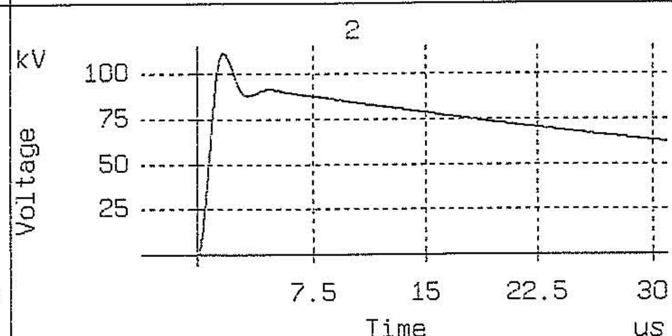
C 50% LI full

55.8kV T1=1.18us T2=--



C 100% LI full

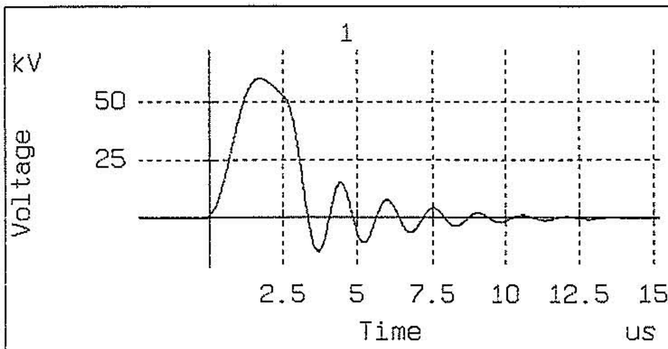
110.2kV T1=1.24us T2=38.8us



C 100% LI full

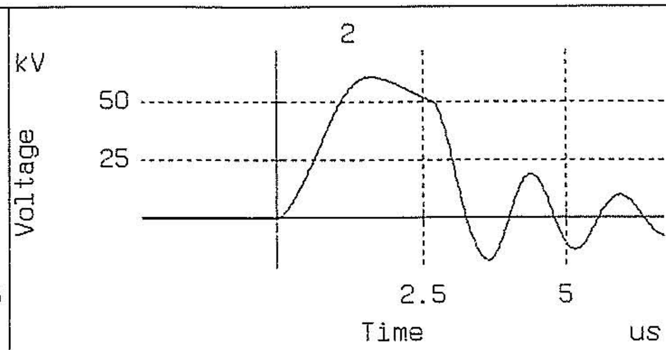
111.5kV T1=1.19us T2=--

12.12.2008



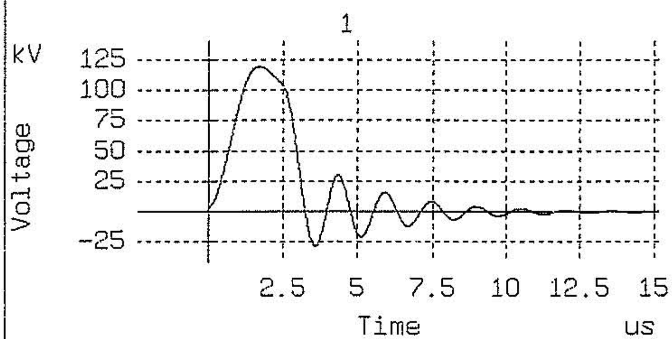
C 50% LI tail chopped

60.29kV -23.71% T1=1.24us Tc=2.41us



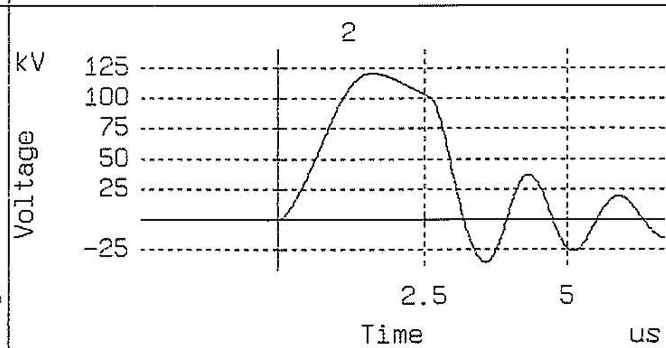
C 50% LI tail chopped

60.84kV -29.52% T1=1.18us Tc=2.5us



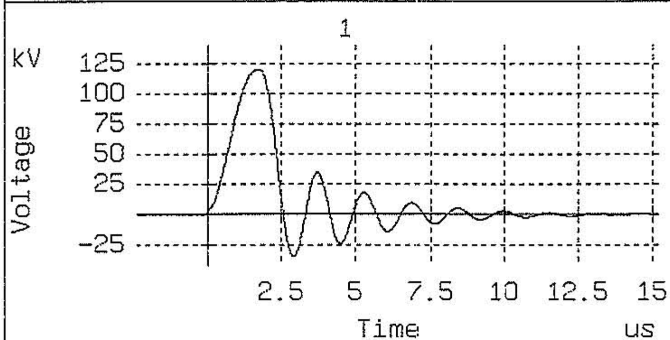
C 100% LI tail chopped

120kV -23.81% T1=1.24us Tc=2.32us



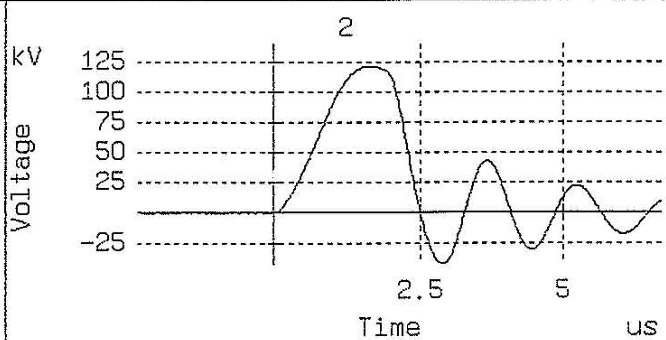
C 100% LI tail chopped

121.3kV -29.2% T1=1.18us Tc=2.45us



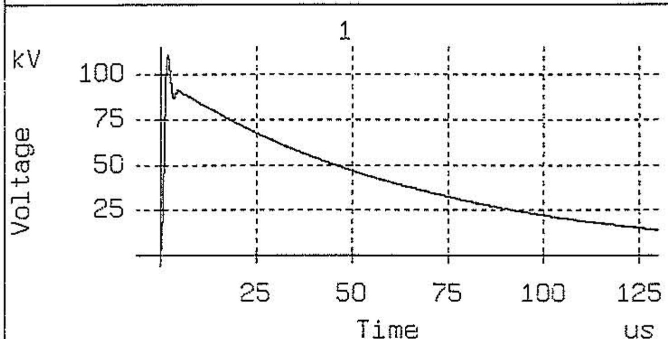
C 100% LI tail chopped

120.1kV -28.95% T1=1.24us Tc=1.68us



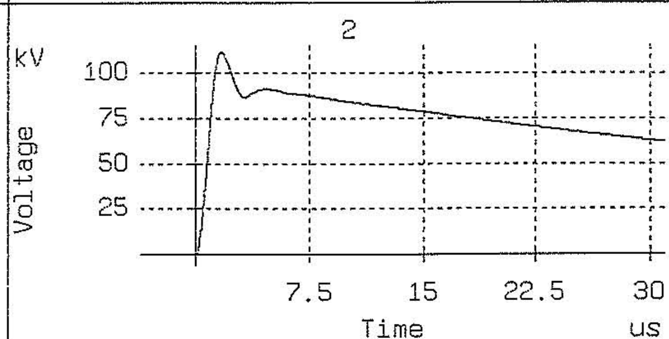
C 100% LI tail chopped

121.2kV -34.49% T1=1.18us Tc=1.76us U



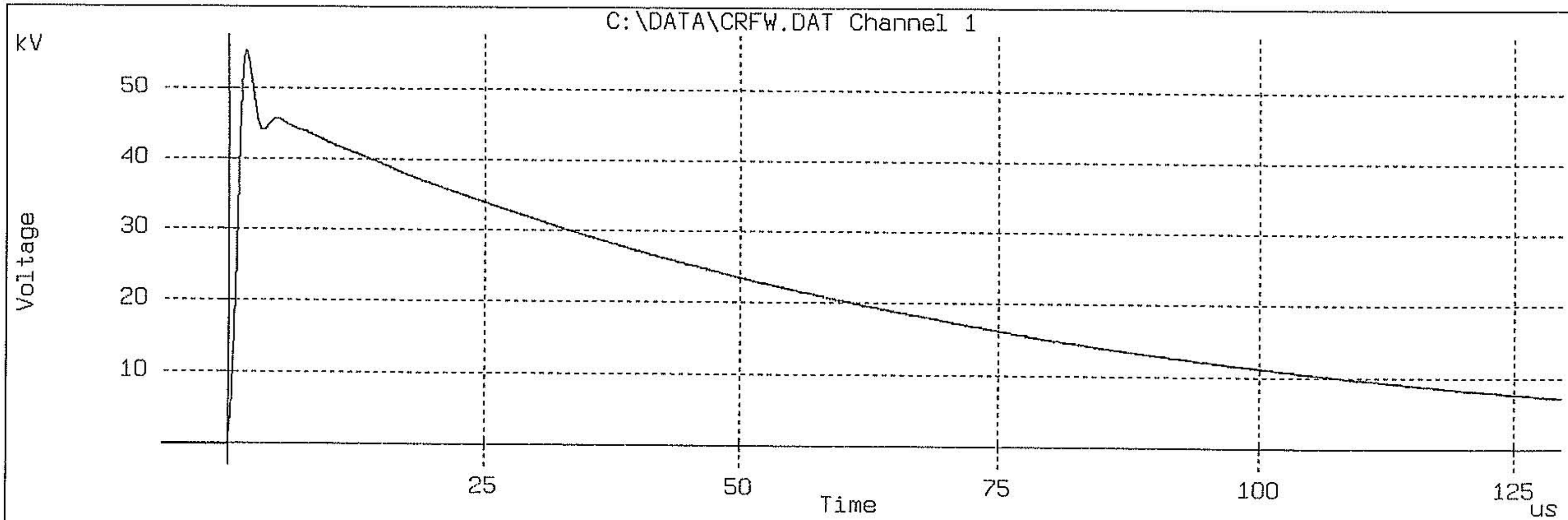
C 100% LI full

110.2kV T1=1.25us T2=38.6us

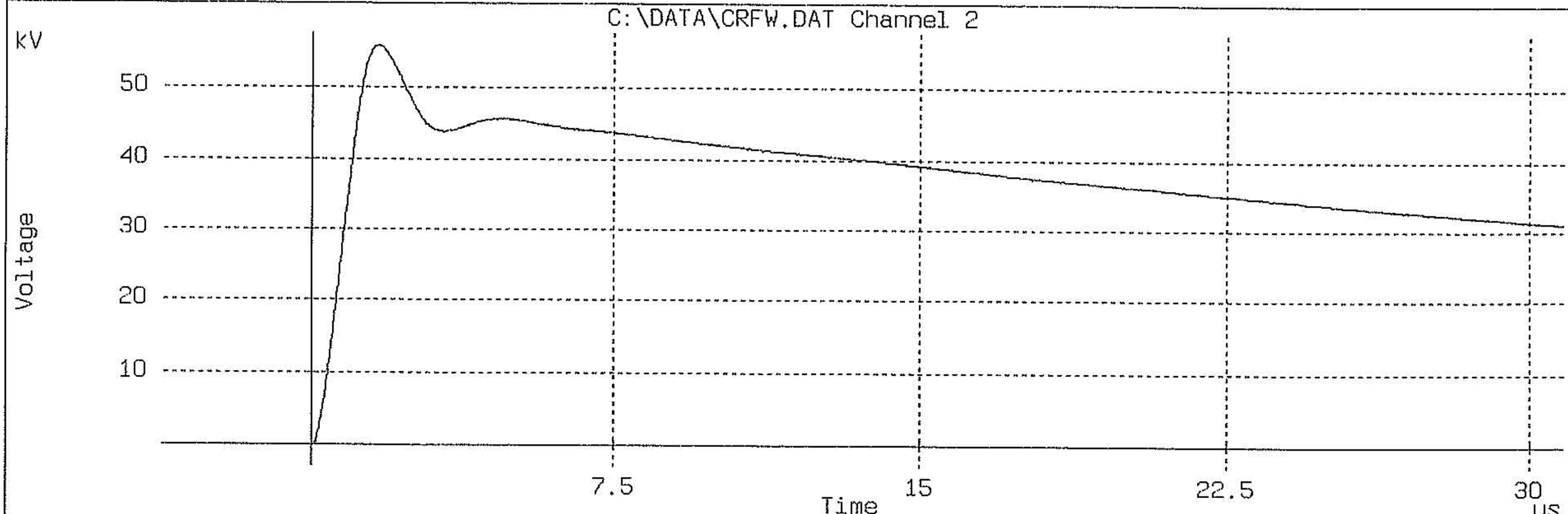


C 100% LI full

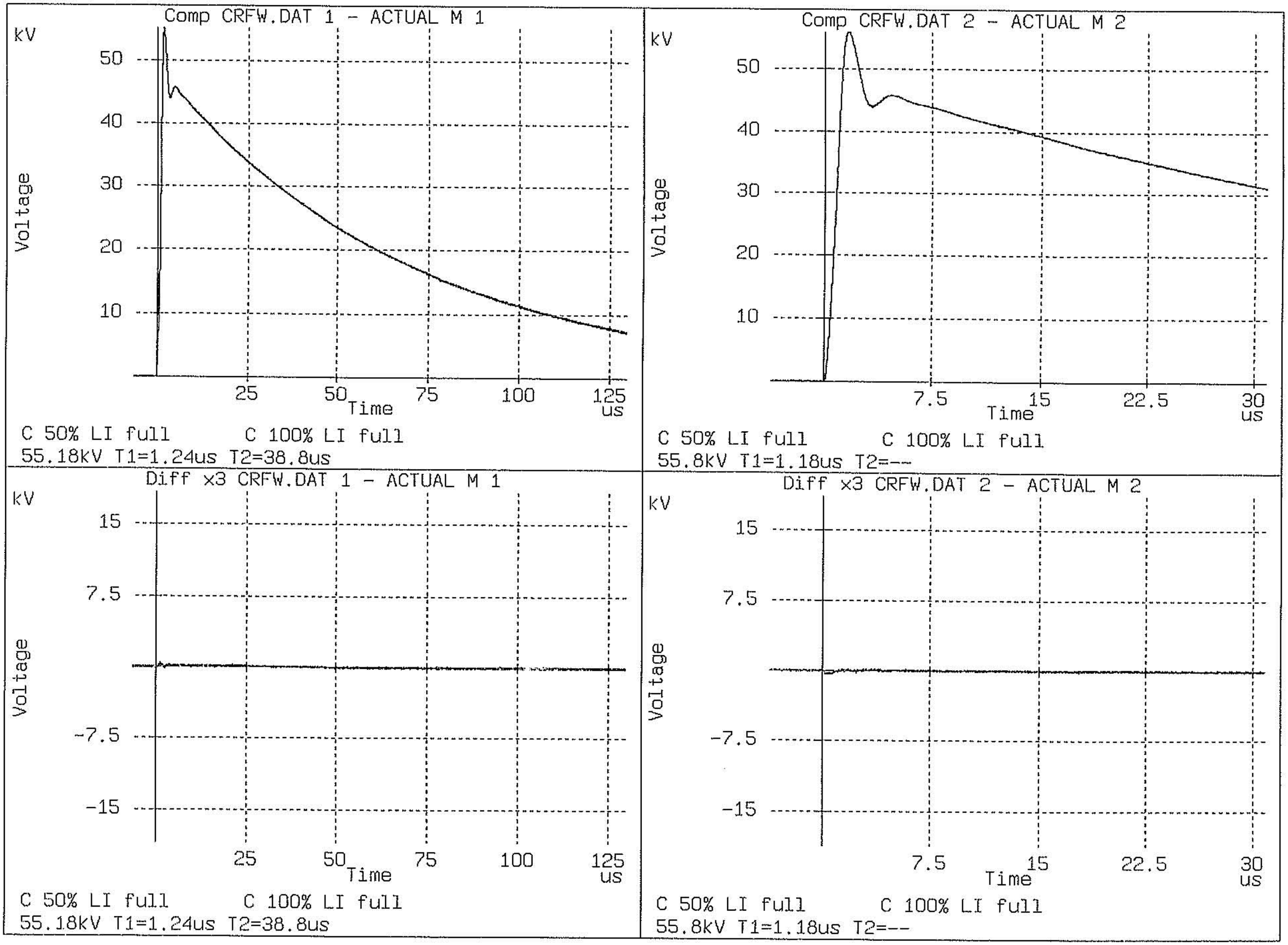
111.5kV T1=1.19us T2=--



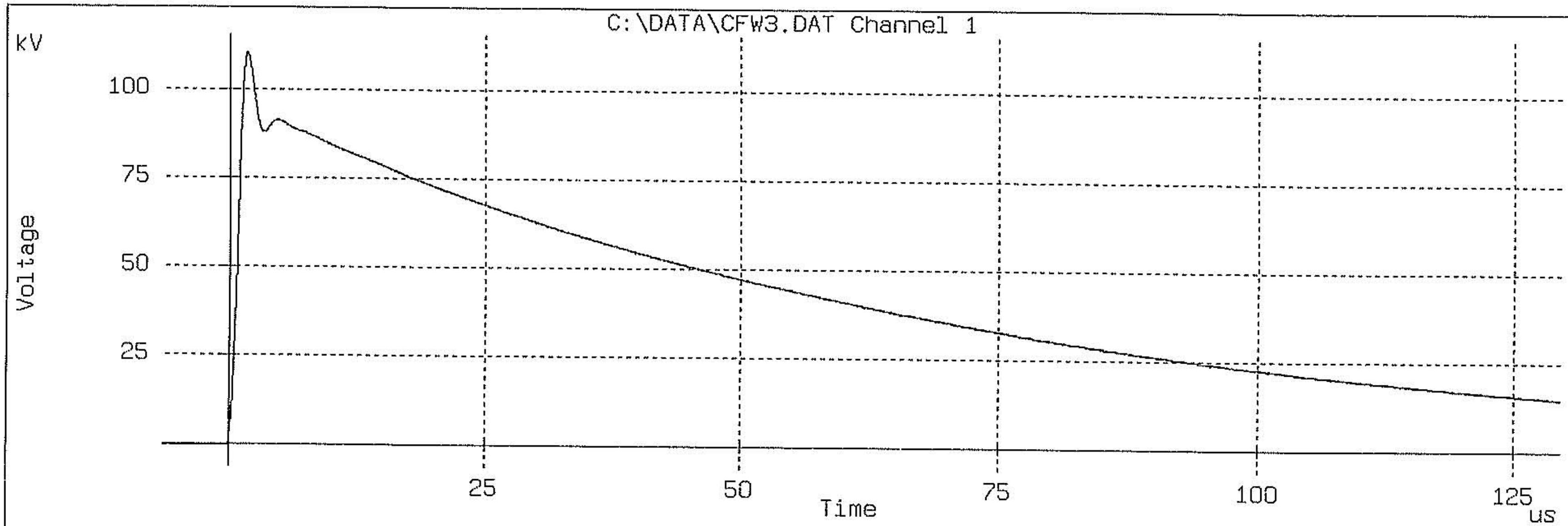
C 50% LI full
55.18kV T1=1.24us T2=38.8us



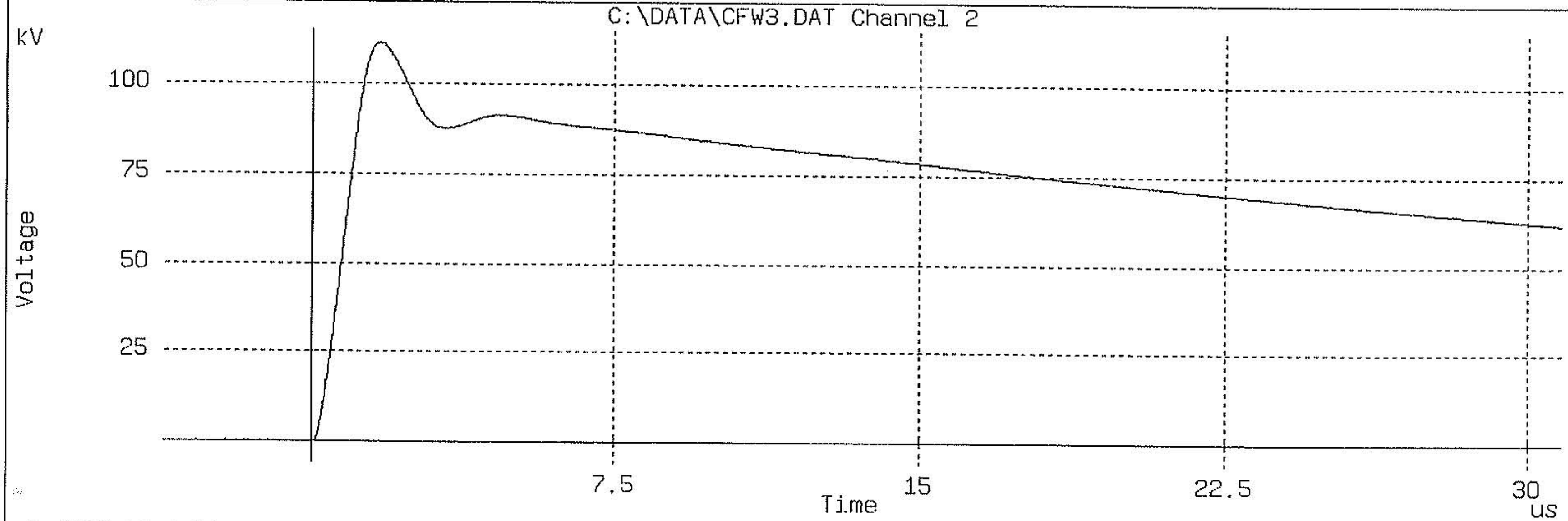
C 50% LI full
55.8kV T1=1.18us T2=--



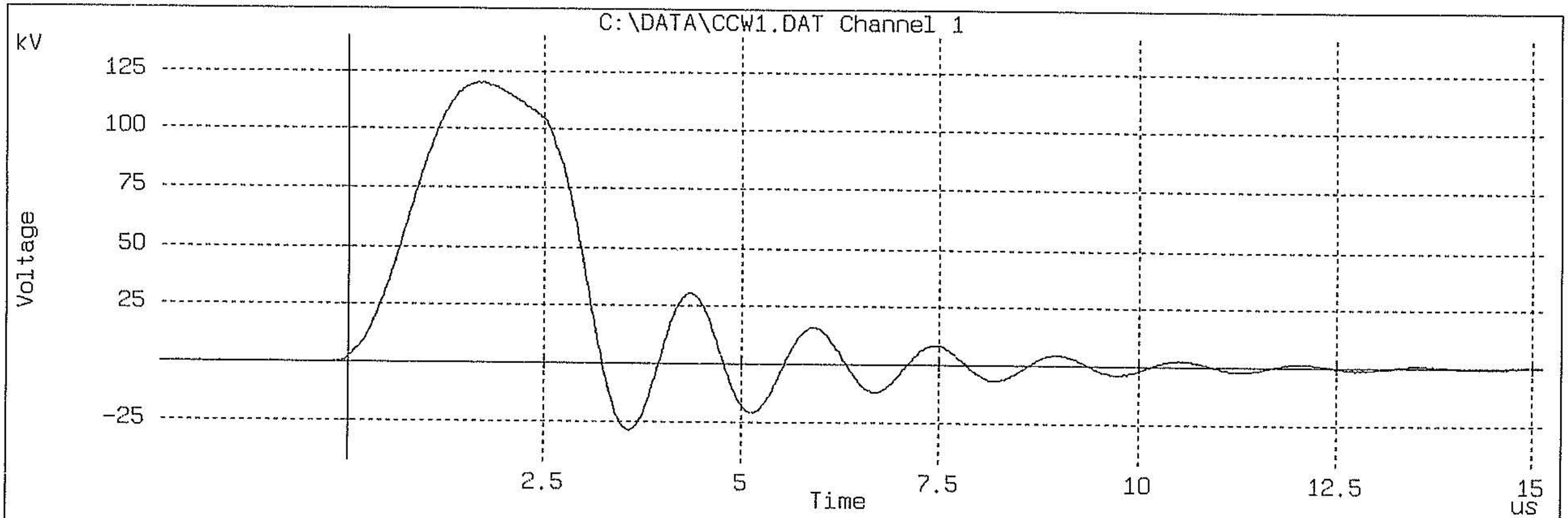
Comp CRFW.DAT 1 - ACTUAL M 1
kV
Voltage
50
40
30
20
10
25
50
75
100
125
us
Time
C 50% LI full
C 100% LI full
55.18kV T1=1.24us T2=38.8us
Comp CRFW.DAT 2 - ACTUAL M 2
kV
Voltage
50
40
30
20
10
7.5
15
22.5
30
us
Time
C 50% LI full
C 100% LI full
55.8kV T1=1.18us T2=--
Diff x3 CRFW.DAT 1 - ACTUAL M 1
kV
Voltage
15
7.5
-7.5
-15
25
50
75
100
125
us
Time
C 50% LI full
C 100% LI full
55.18kV T1=1.24us T2=38.8us
Diff x3 CRFW.DAT 2 - ACTUAL M 2
kV
Voltage
15
7.5
-7.5
-15
7.5
15
22.5
30
us
Time
C 50% LI full
C 100% LI full
55.8kV T1=1.18us T2=--



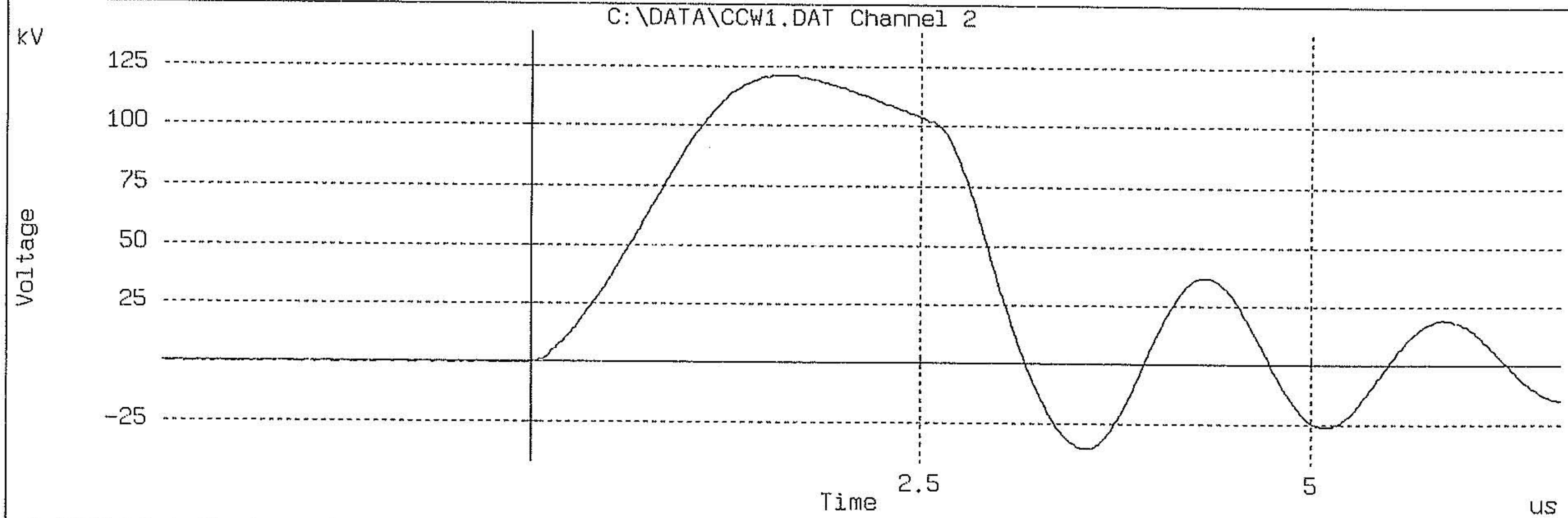
C 100% LI full
110.3kV T1=1.25us T2=38.8us



C 100% LI full
111.6kV T1=1.19us T2=--

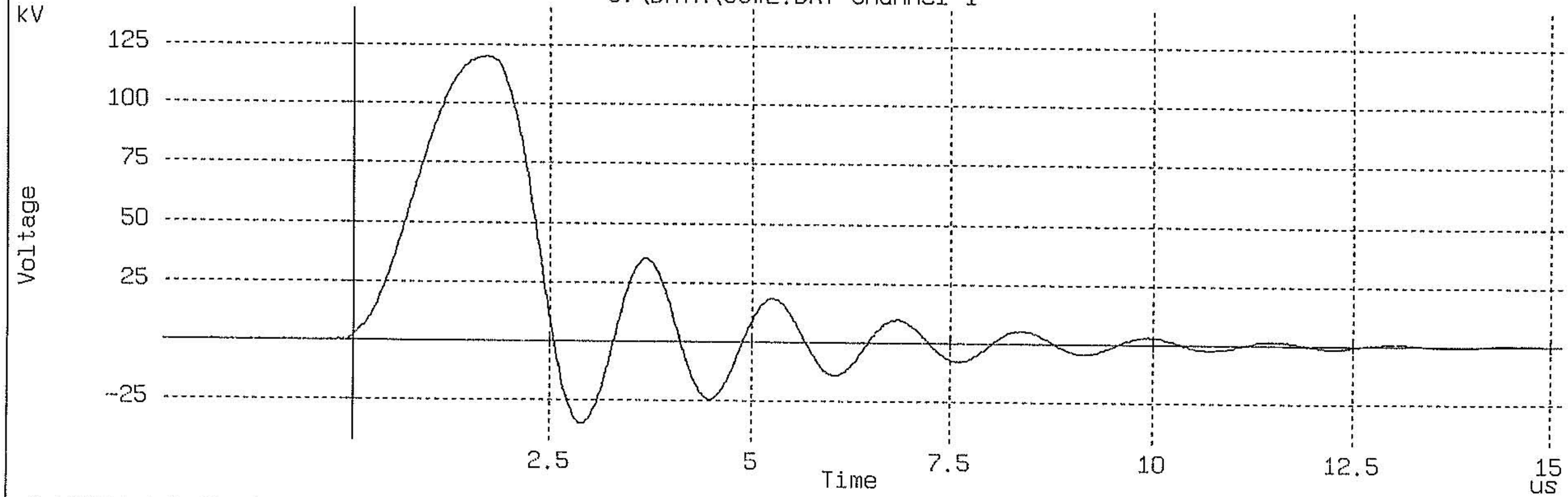


C 100% LI tail chopped
120kV -23.81% T1=1.24us Tc=2.32us



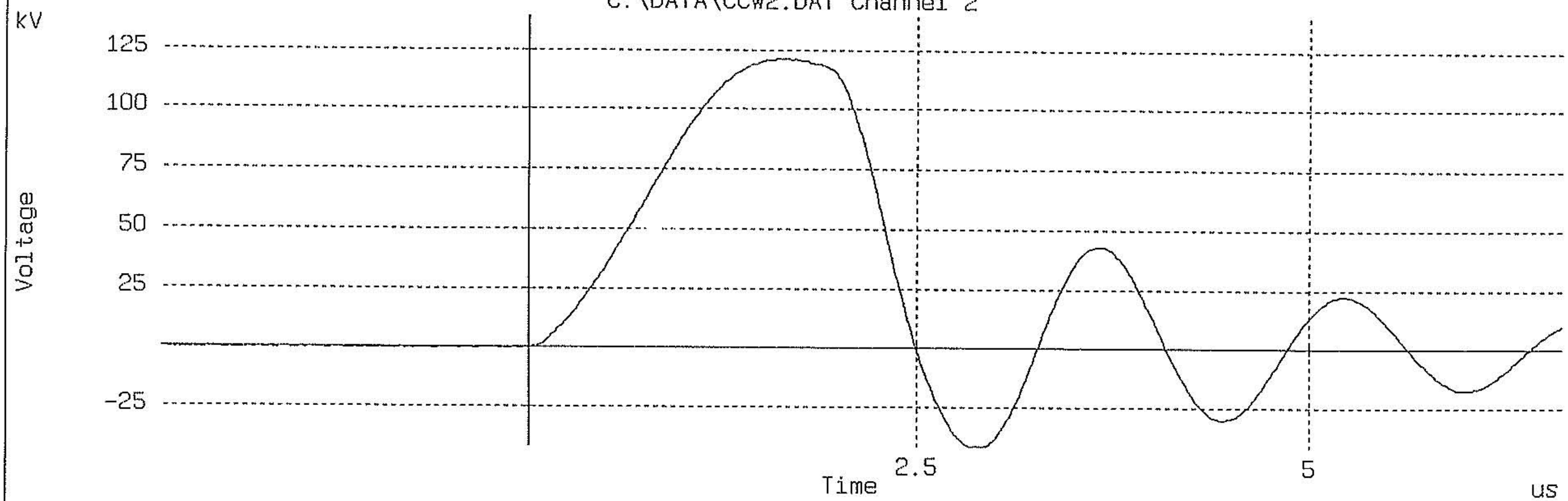
C 100% LI tail chopped
121.3kV -29.2% T1=1.18us Tc=2.45us

C:\DATA\CCW2.DAT Channel 1

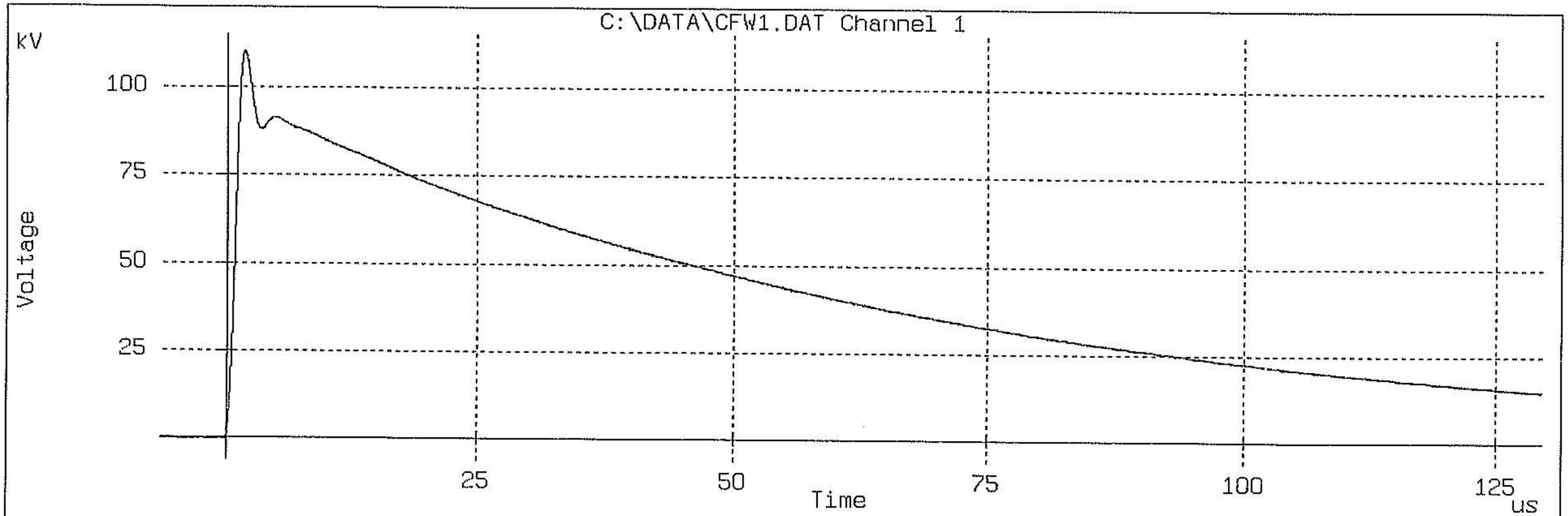


C 100% LI tail chopped
120.1kV -28.95% T1=1.24us Tc=1.68us

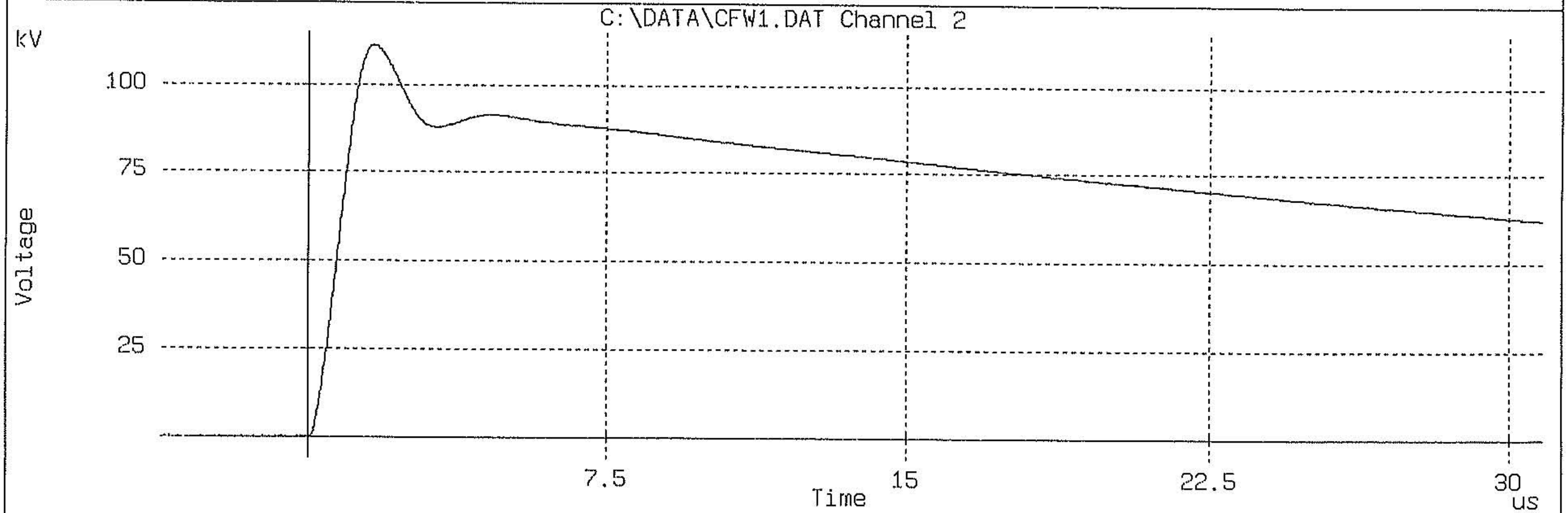
C:\DATA\CCW2.DAT Channel 2



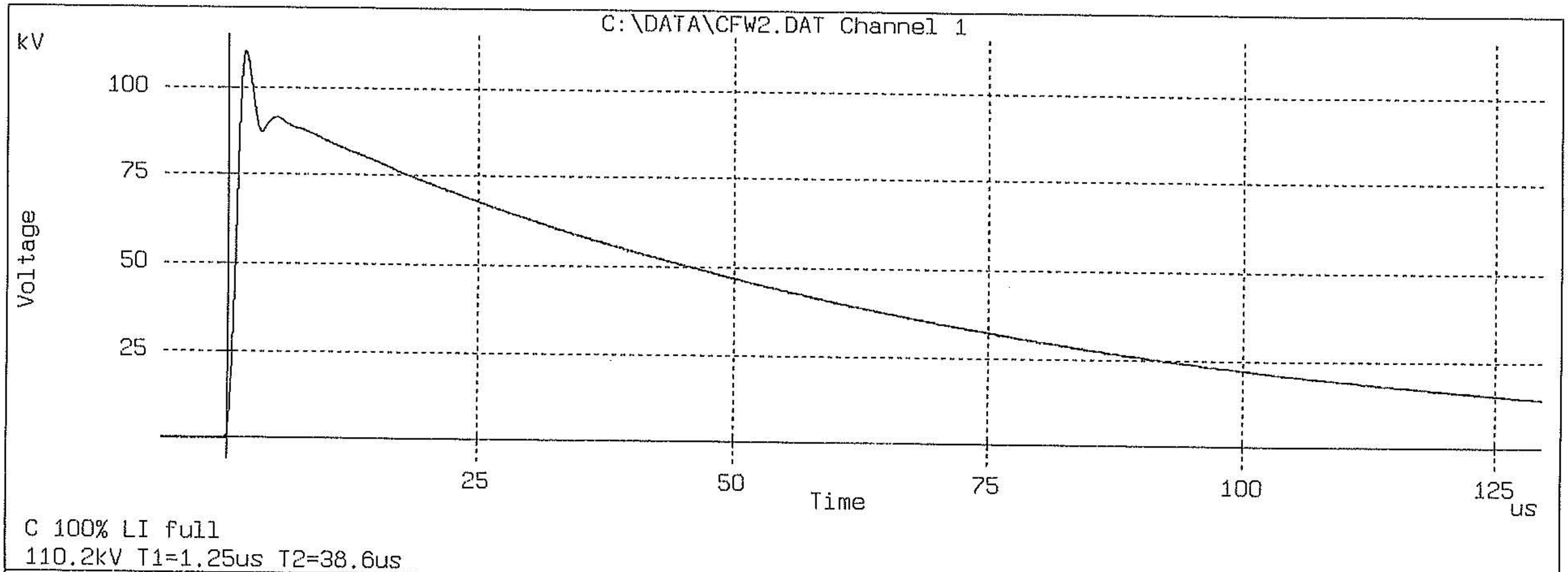
C 100% LI tail chopped
121.2kV -34.49% T1=1.18us Tc=1.76us Underflow

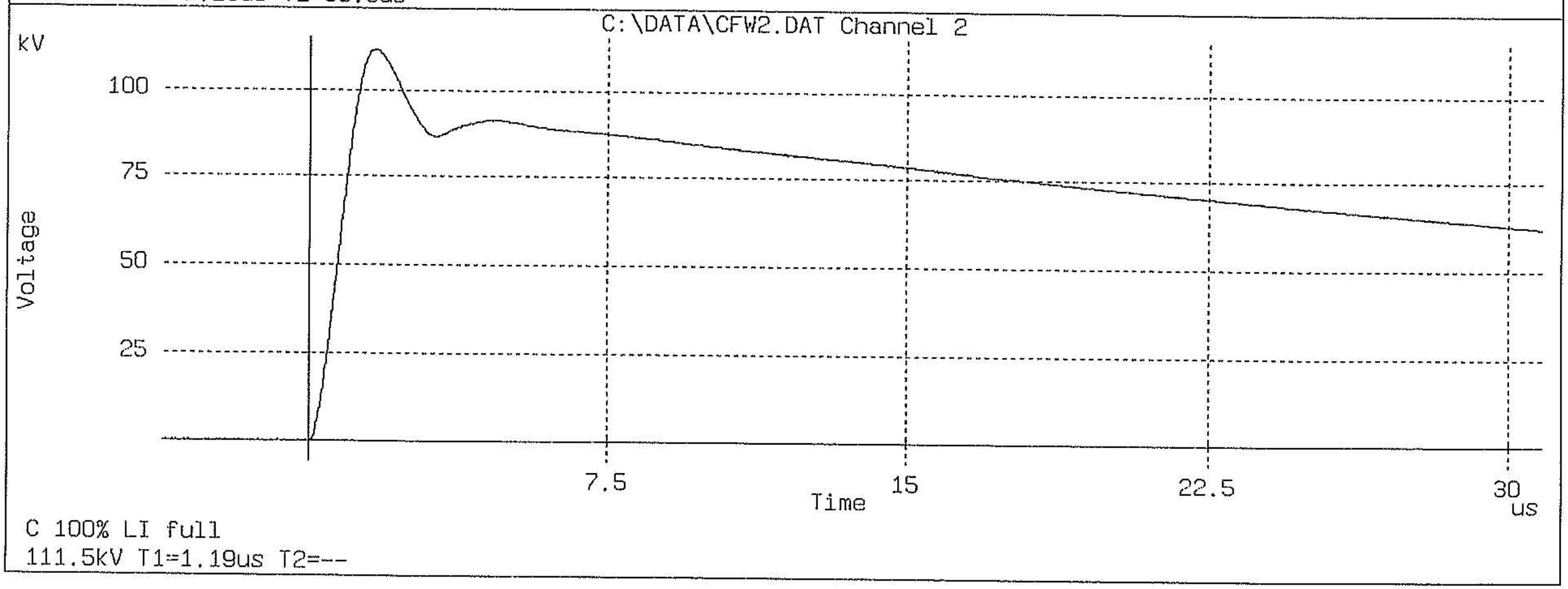


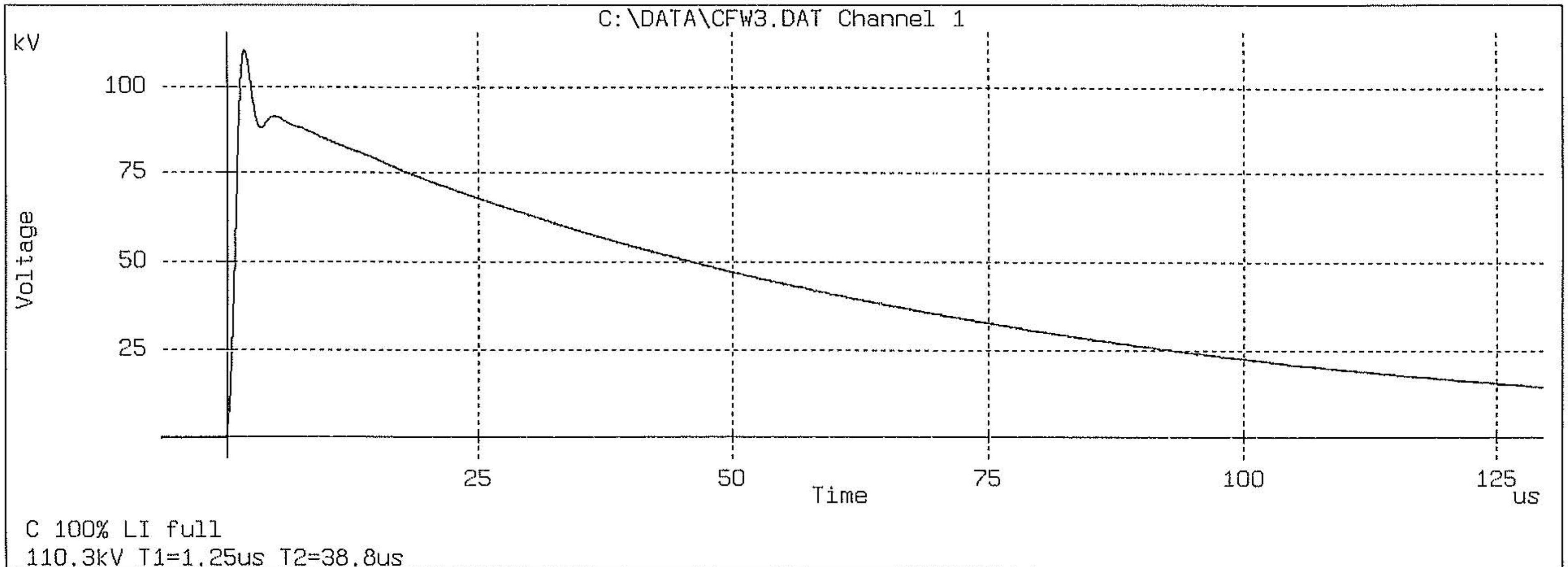
C 100% LI full
110.2kV T1=1.24us T2=38.8us

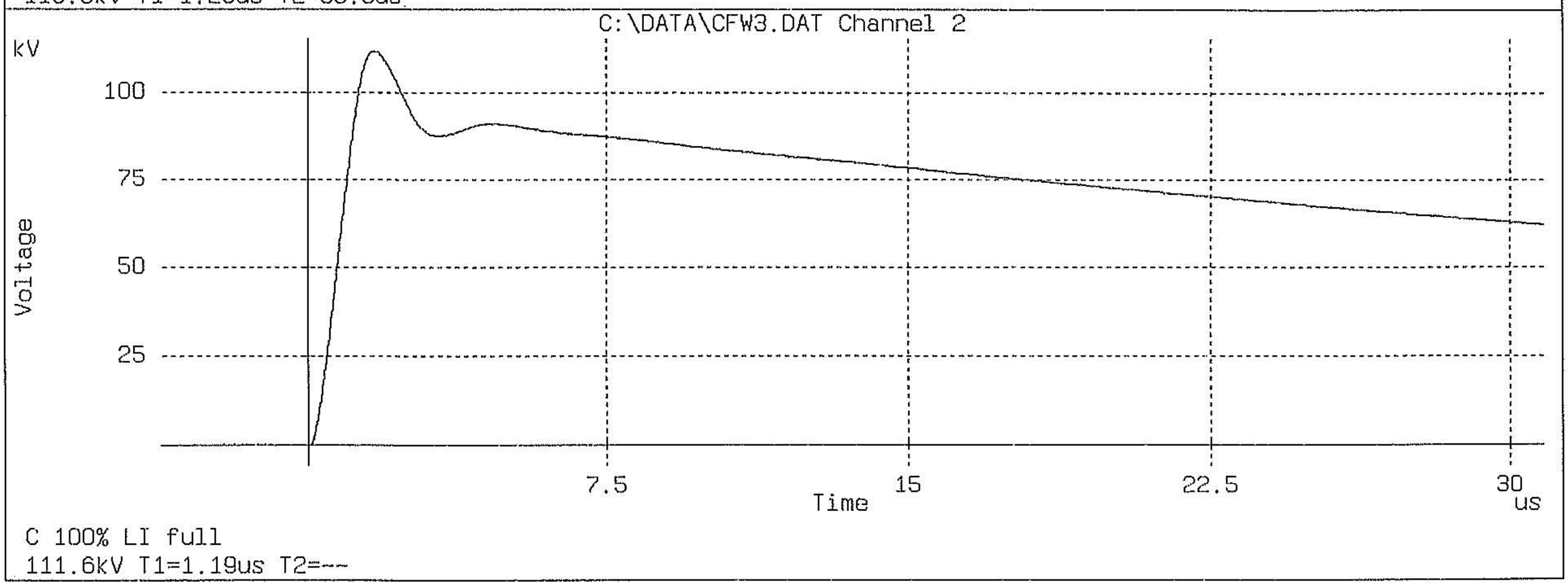


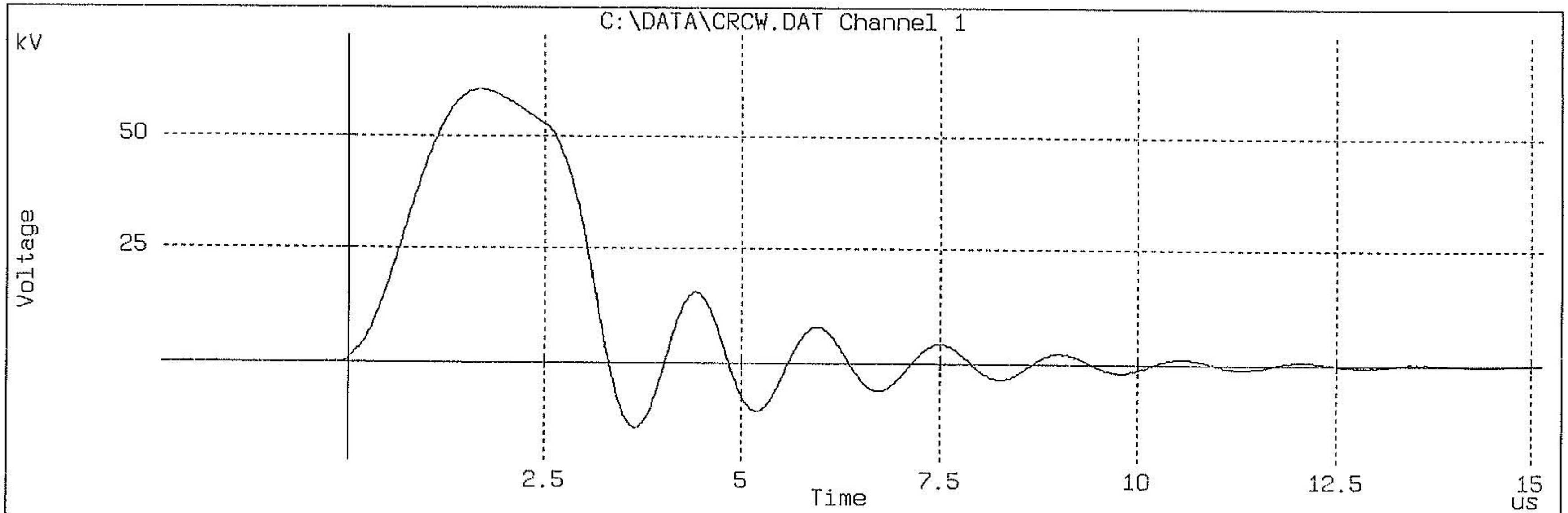
C 100% LI full
111.5kV T1=1.19us T2=--


C:\DATA\CFW2.DAT Channel 1
kV
Voltage
100
75
50
25
25
50
75
100
125
us
Time
C 100% LI full
110.2kV T1=1.25us T2=38.6us

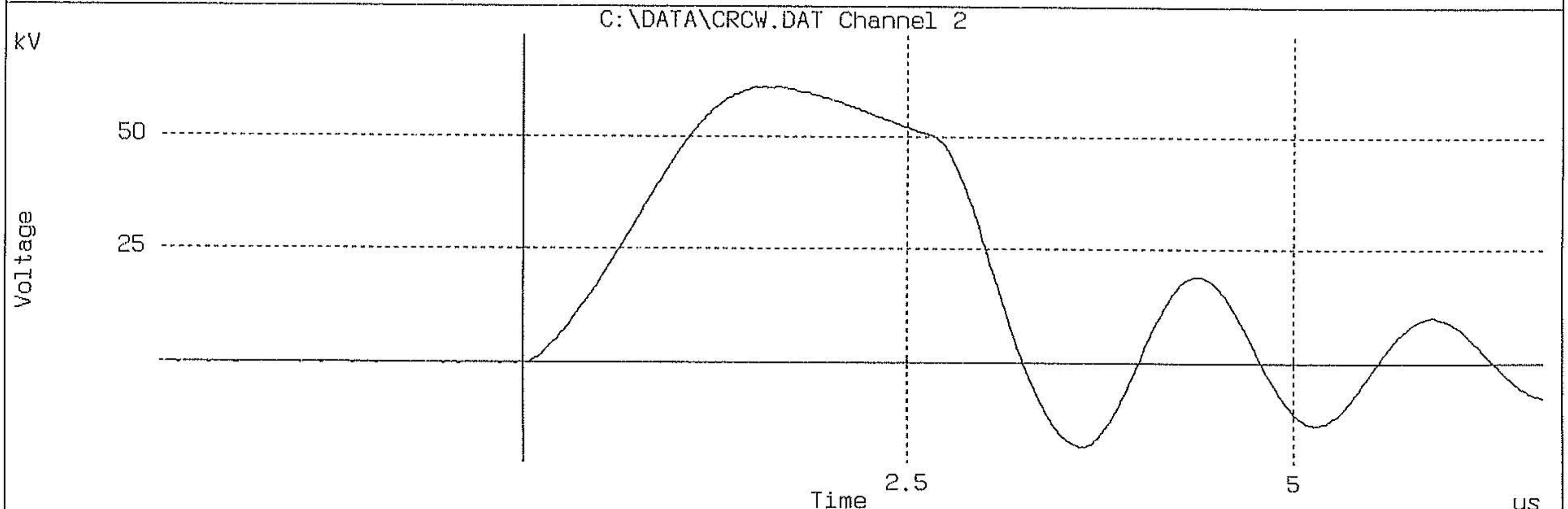

C:\DATA\CFW2.DAT Channel 2
kV
Voltage
100
75
50
25
7.5
15
22.5
30
us
Time
C 100% LI full
111.5kV T1=1.19us T2=--


C:\DATA\CFW3.DAT Channel 1
kV
Voltage
100
75
50
25
25
50
75
100
125
Time
us
C 100% LI full
110.3kV T1=1.25us T2=38.8us

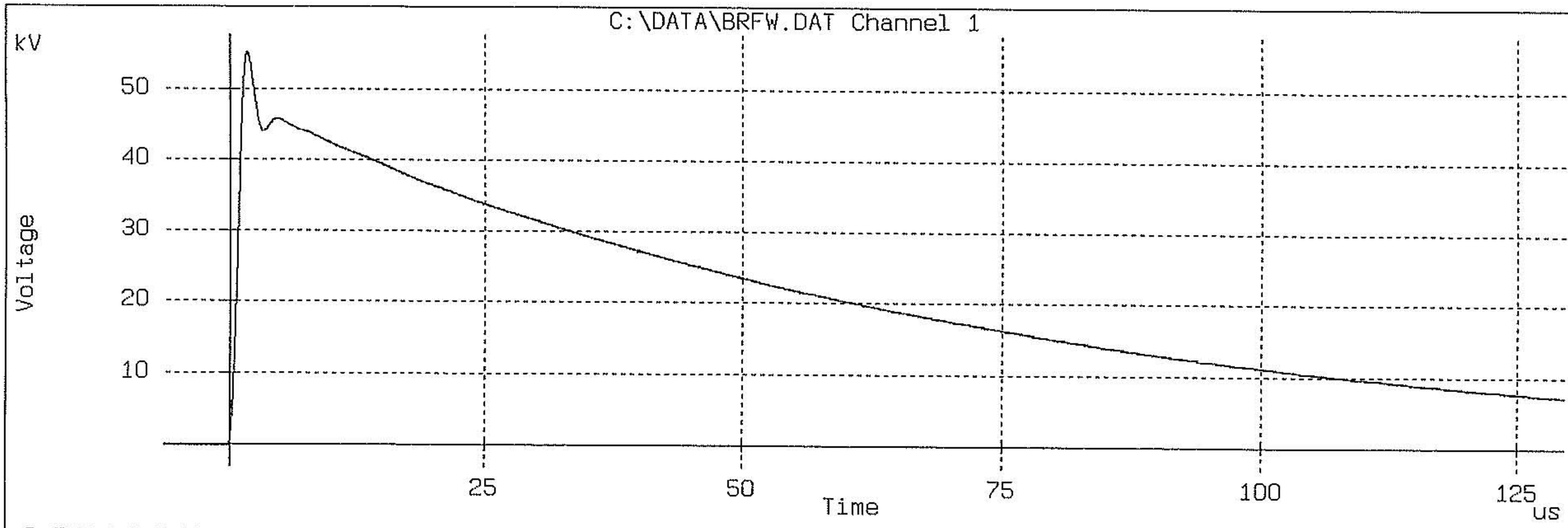

C:\DATA\CFW3.DAT Channel 2
kV
Voltage
100
75
50
25
7.5
15
22.5
30
Time
us
C 100% LI full
111.6kV T1=1.19us T2=--



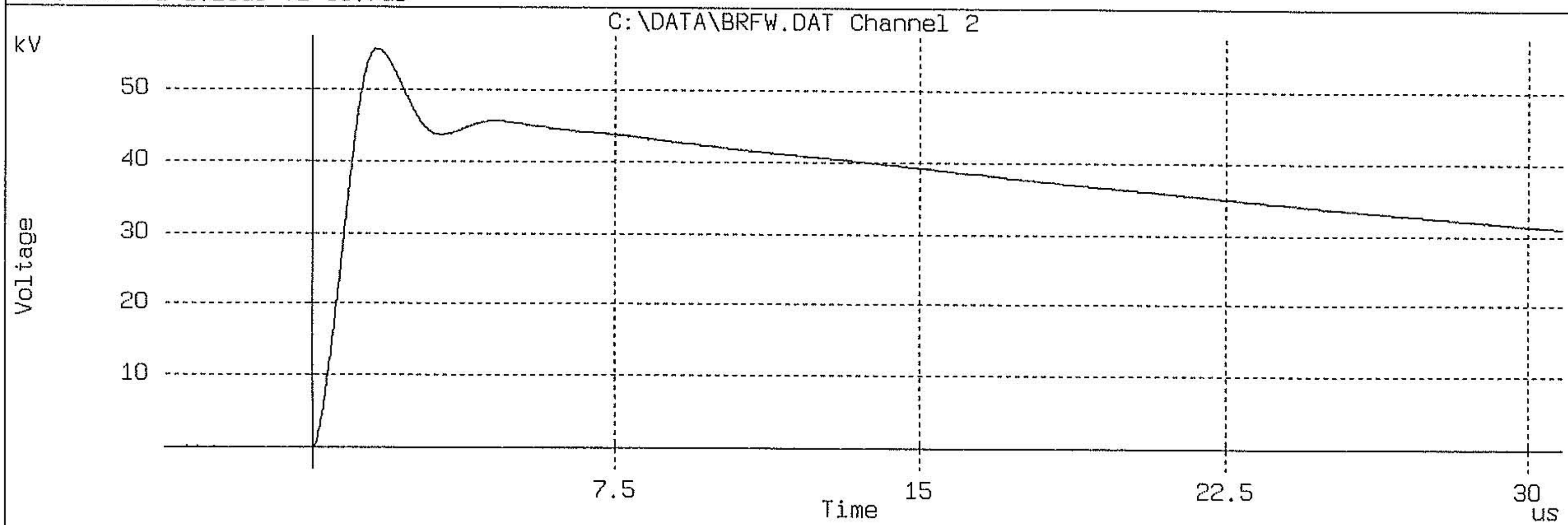
C 50% LI tail chopped
60.29kV -23.71% T1=1.24us Tc=2.41us



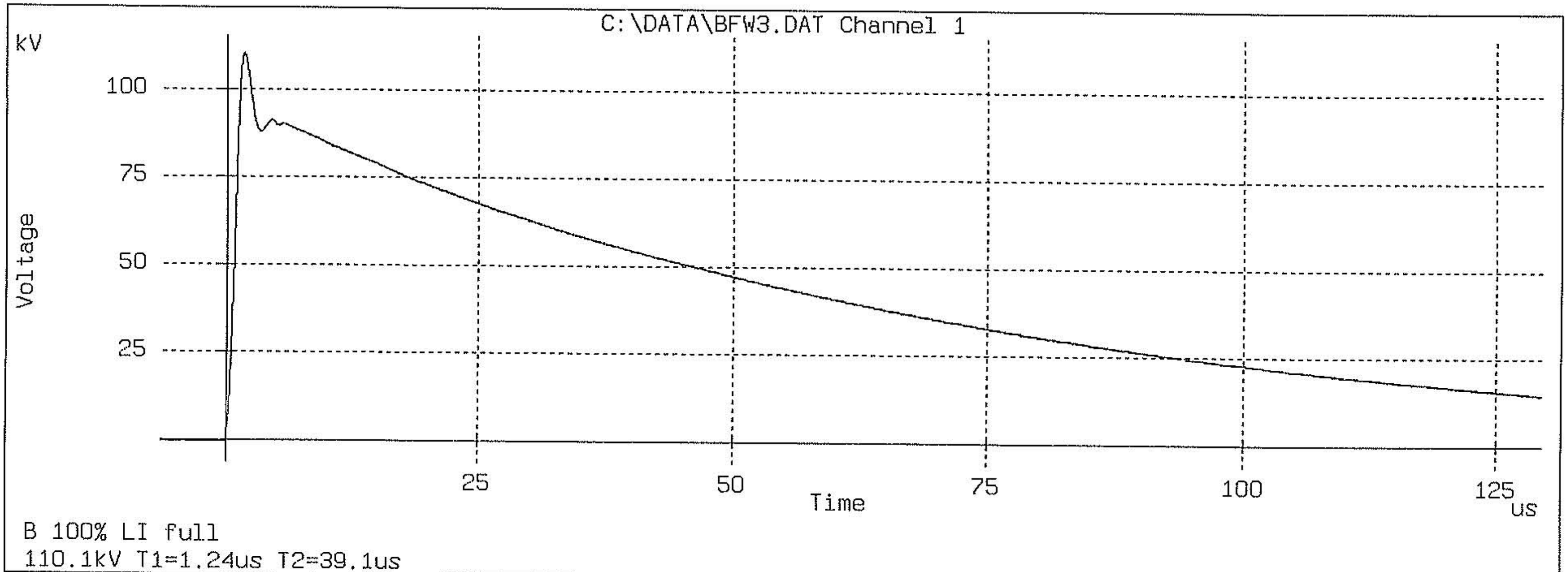
C 50% LI tail chopped
60.84kV -29.52% T1=1.18us Tc=2.5us

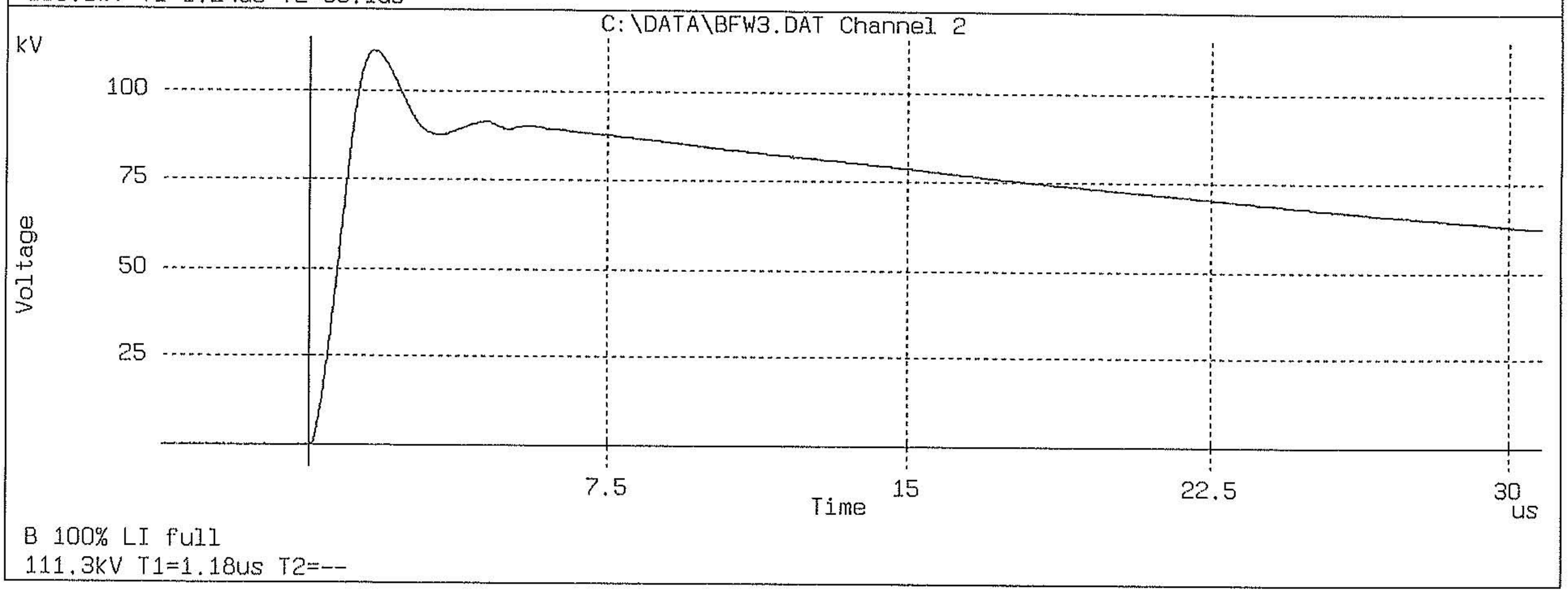


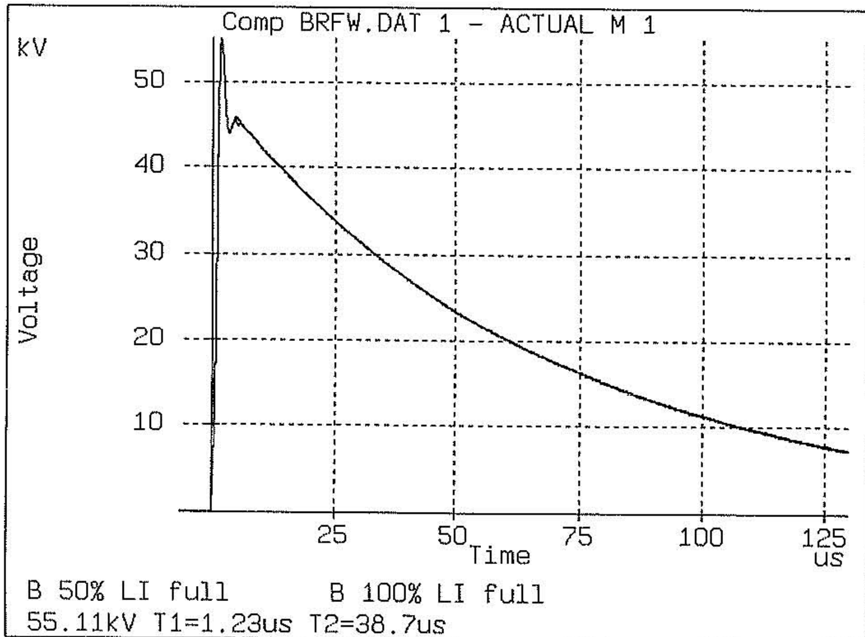
B 50% LI full
55.11kV T1=1.23us T2=38.7us



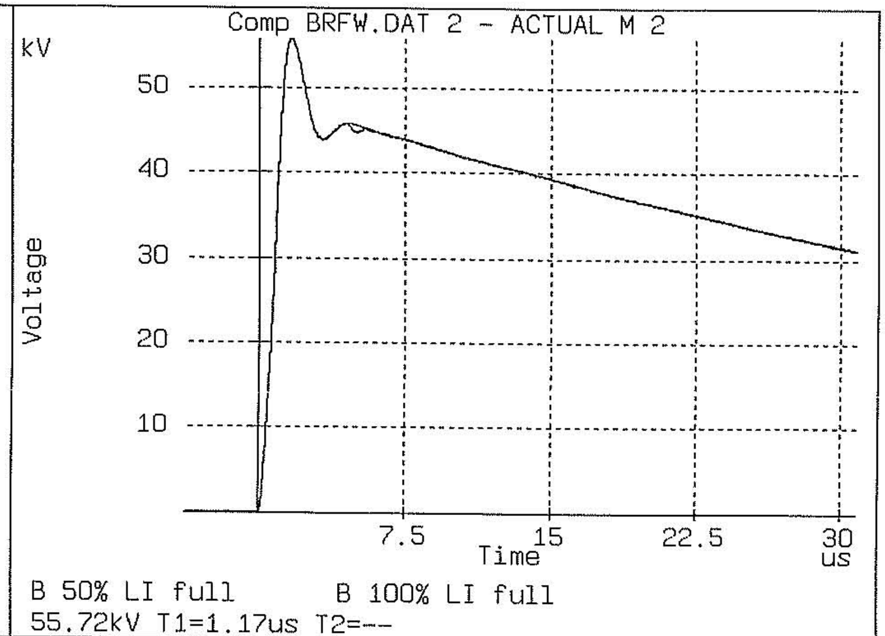
B 50% LI full
55.72kV T1=1.17us T2=--


C:\DATA\BFW3.DAT Channel 1
kV
Voltage
100
75
50
25
25
50
75
100
125
us
Time
B 100% LI full
110.1kV T1=1.24us T2=39.1us

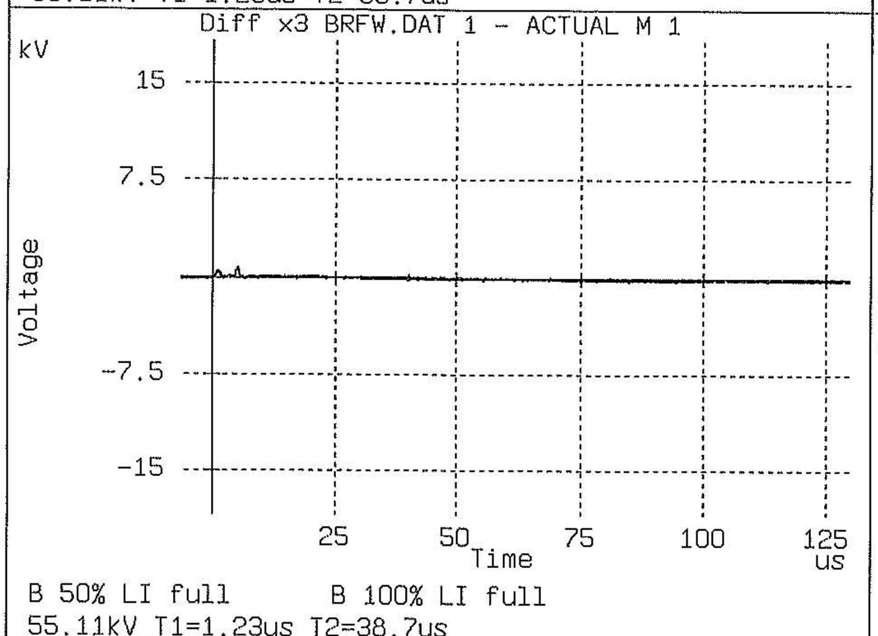

C:\DATA\BFW3.DAT Channel 2
kV
Voltage
100
75
50
25
7.5
15
22.5
30
us
Time
B 100% LI full
111.3kV T1=1.18us T2=--



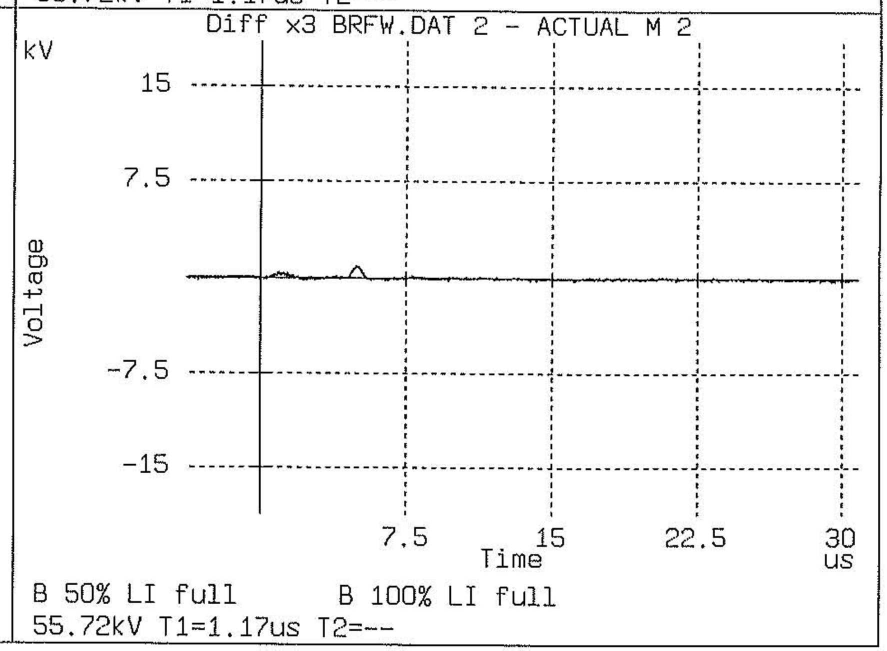
Comp BRFW.DAT 1 - ACTUAL M 1
kV
Voltage
50
40
30
20
10
25
50
75
100
125
us
Time
B 50% LI full
B 100% LI full
55.11kV T1=1.23us T2=38.7us



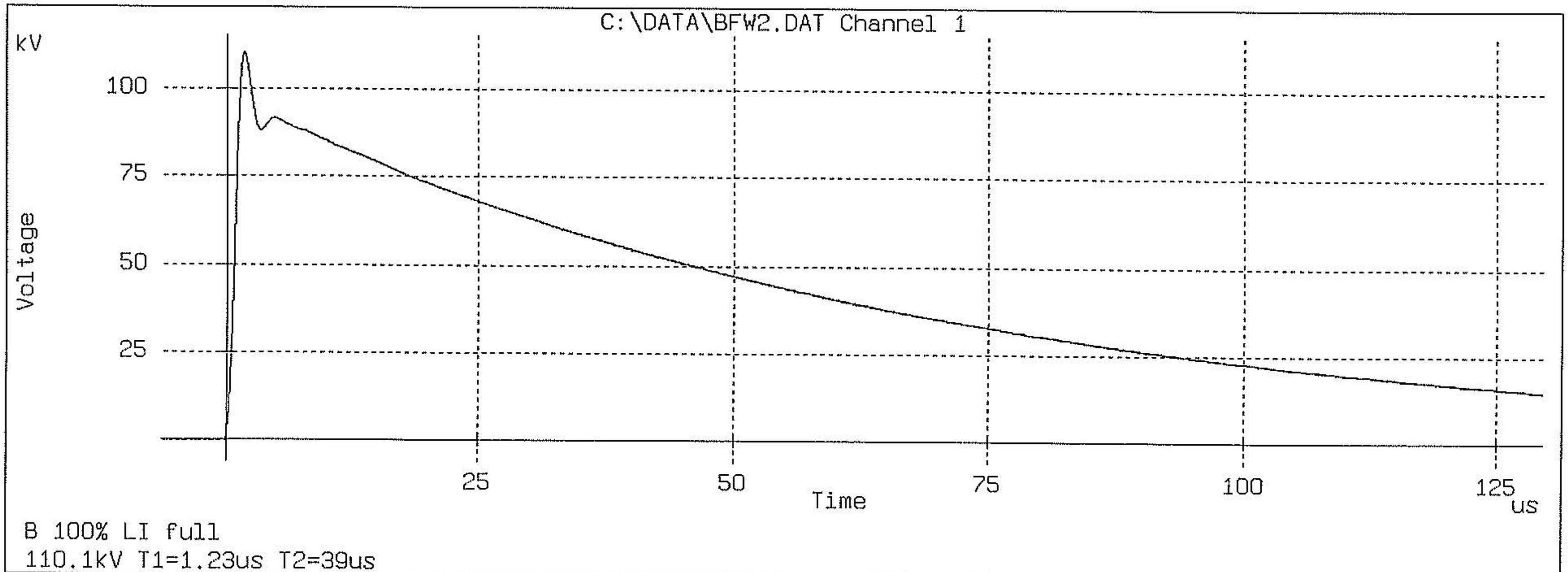
Comp BRFW.DAT 2 - ACTUAL M 2
kV
Voltage
50
40
30
20
10
7.5
15
22.5
30
us
Time
B 50% LI full
B 100% LI full
55.72kV T1=1.17us T2=--

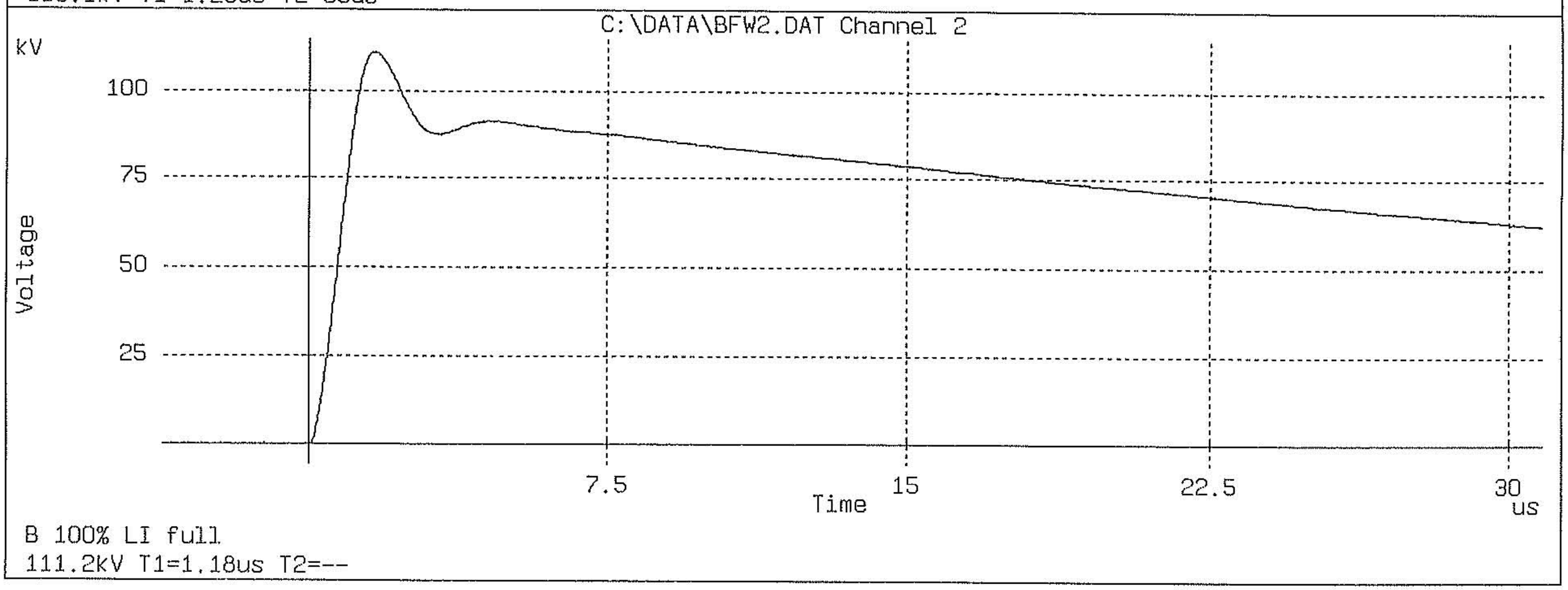


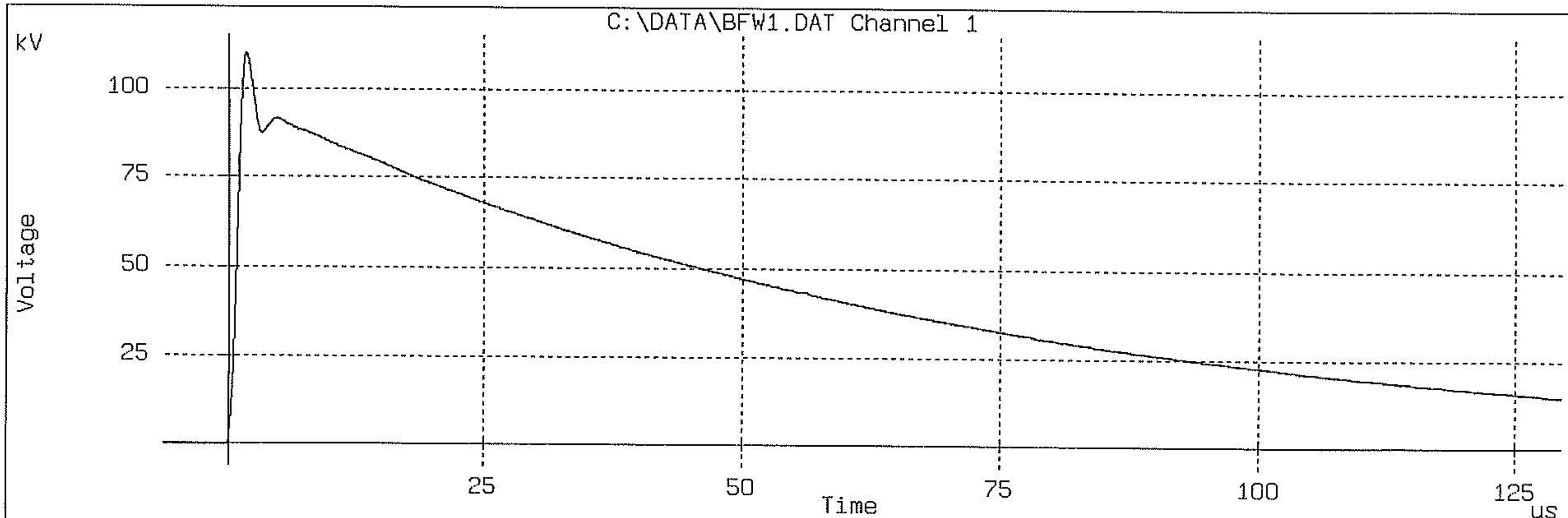
Diff x3 BRFW.DAT 1 - ACTUAL M 1
kV
Voltage
15
7.5
-7.5
-15
25
50
75
100
125
us
Time
B 50% LI full
B 100% LI full
55.11kV T1=1.23us T2=38.7us



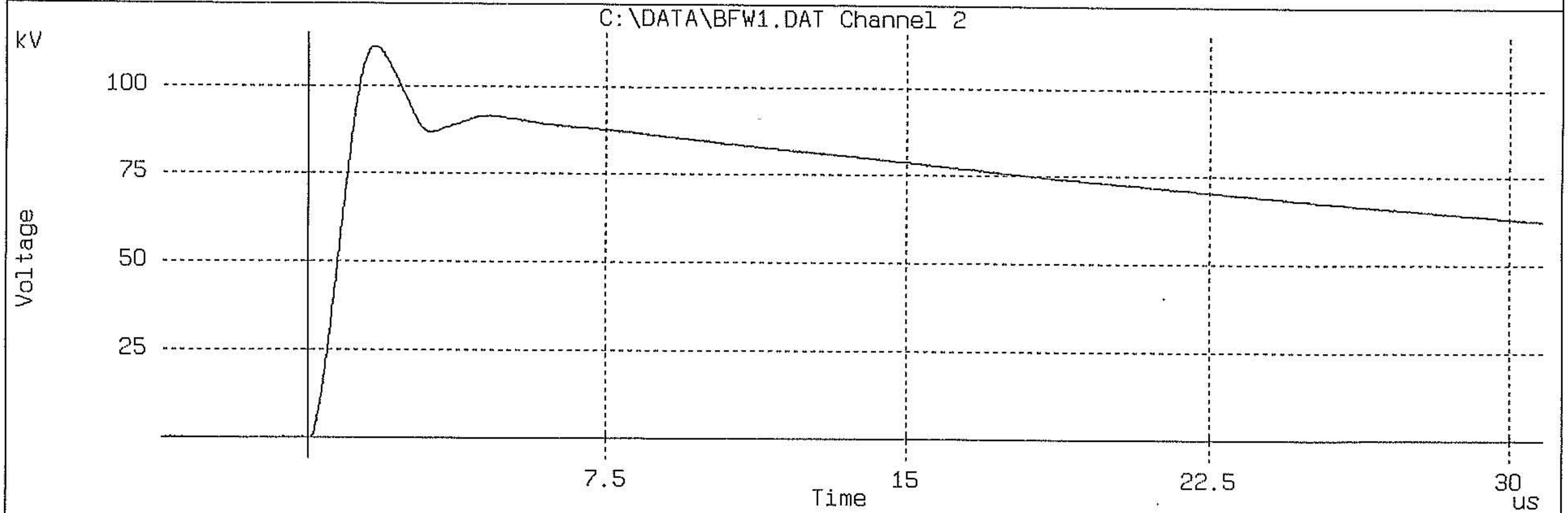
Diff x3 BRFW.DAT 2 - ACTUAL M 2
kV
Voltage
15
7.5
-7.5
-15
7.5
15
22.5
30
us
Time
B 50% LI full
B 100% LI full
55.72kV T1=1.17us T2=--


C:\DATA\BFW2.DAT Channel 1
kV
Voltage
100
75
50
25
25
50
75
100
125
us
Time
B 100% LI full
110.1kV T1=1.23us T2=39us

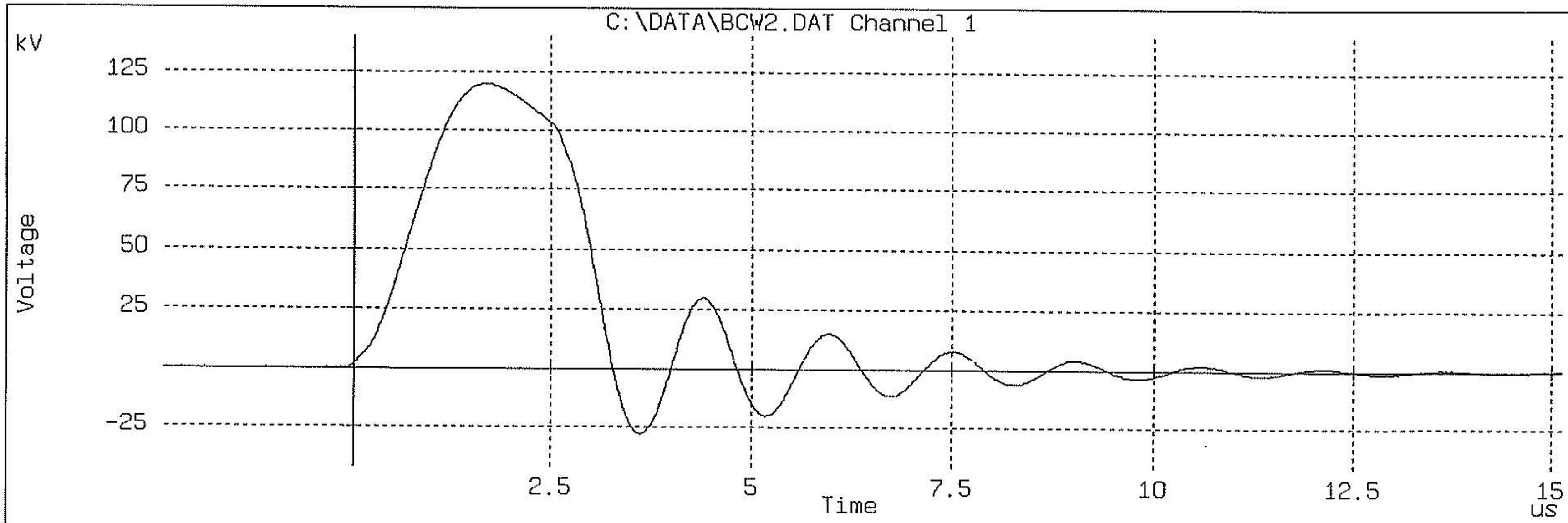

C:\DATA\BFW2.DAT Channel 2
kV
Voltage
100
75
50
25
7.5
15
22.5
30
us
Time
B 100% LI full
111.2kV T1=1.18us T2=--



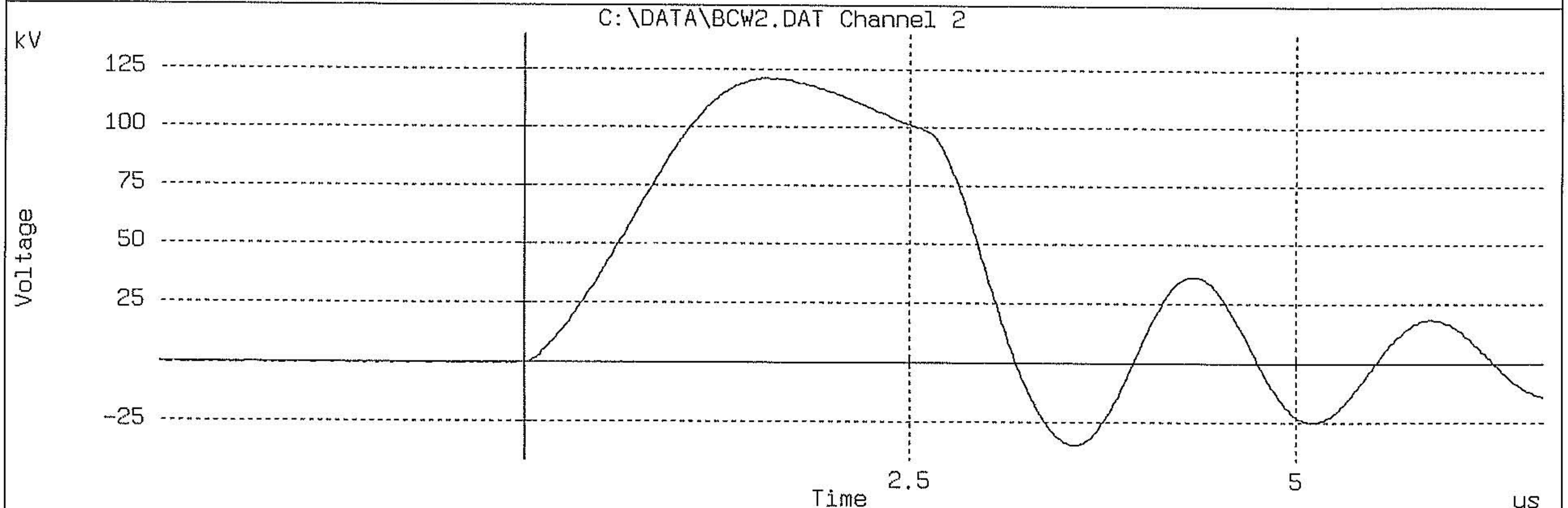
B 100% LI full
110kV T1=1.23us T2=39us



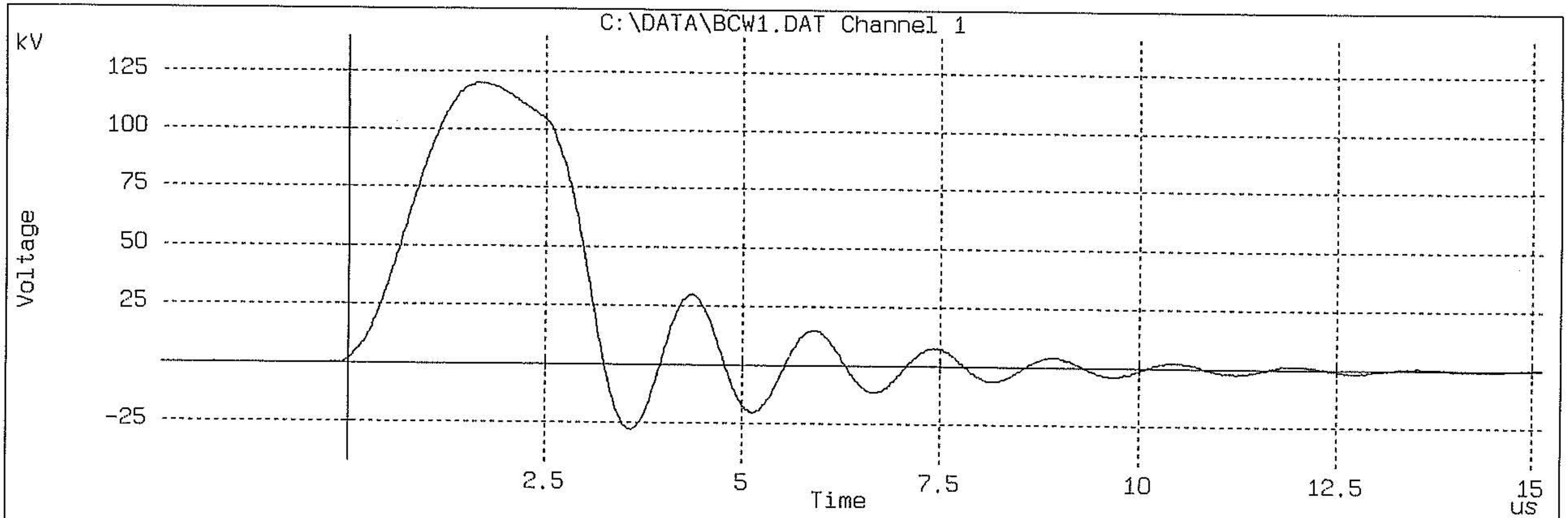
B 100% LI full
111.2kV T1=1.17us T2=--



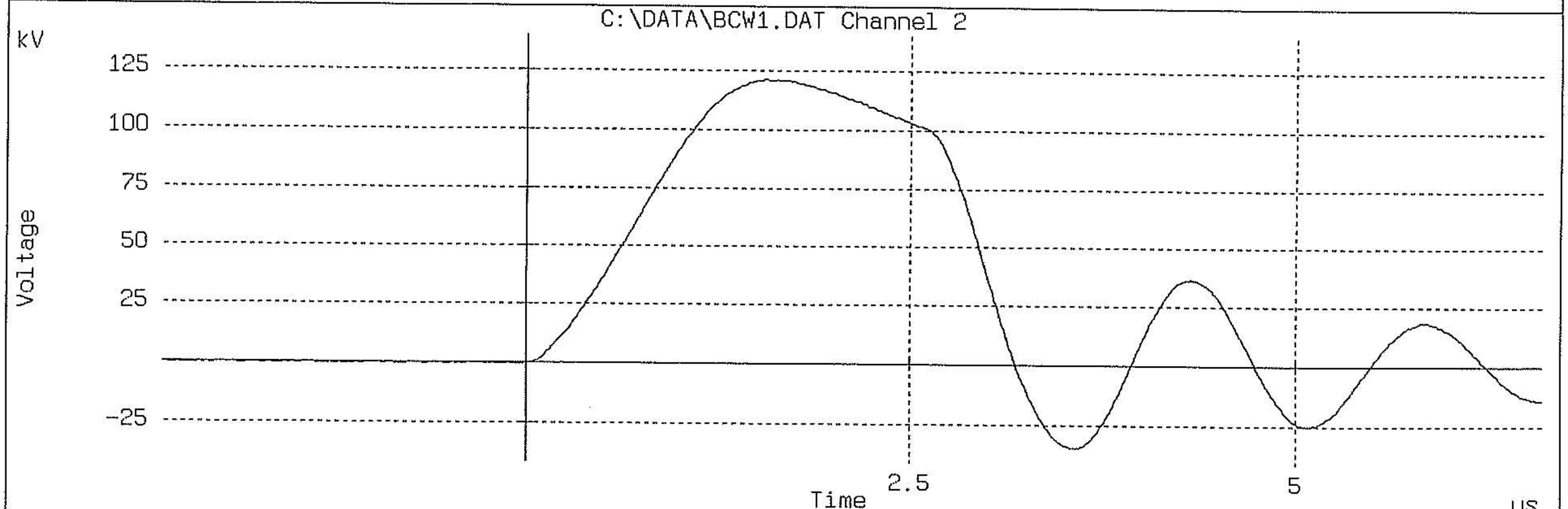
B 100% LI tail chopped
119.8kV -23.55% T1=1.23us Tc=2.34us



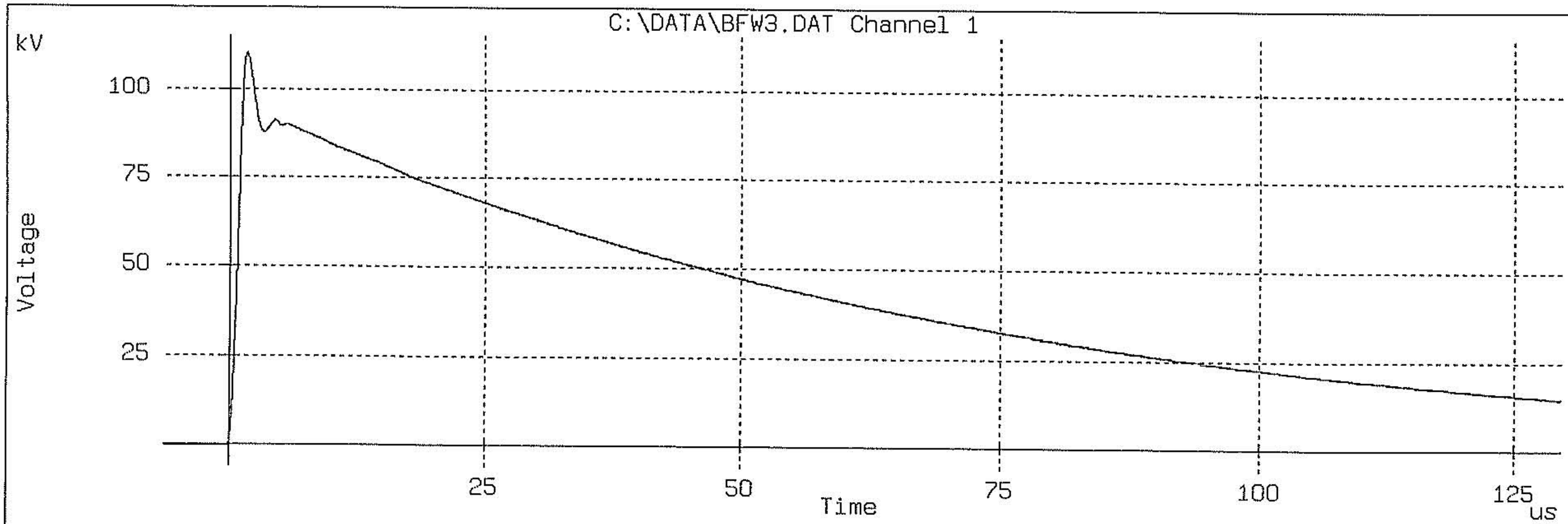
B 100% LI tail chopped
121.2kV -28.66% T1=1.18us Tc=2.46us



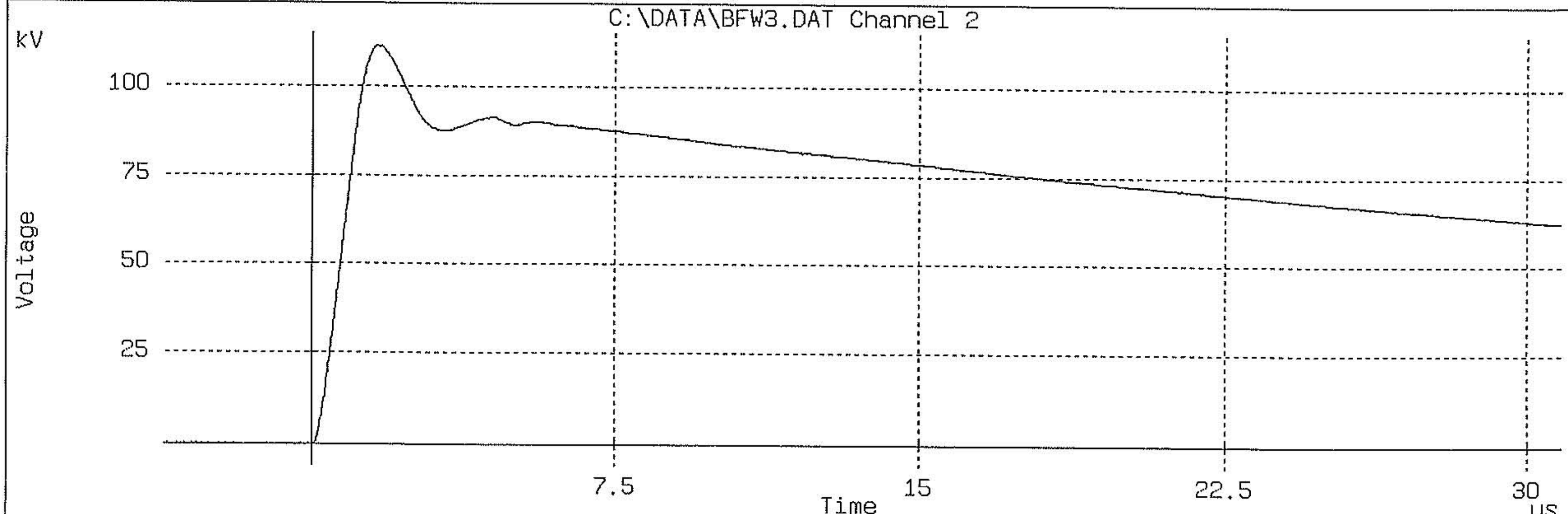
B 100% LI tail chopped
119.9kV -23.3% T1=1.23us Tc=2.34us



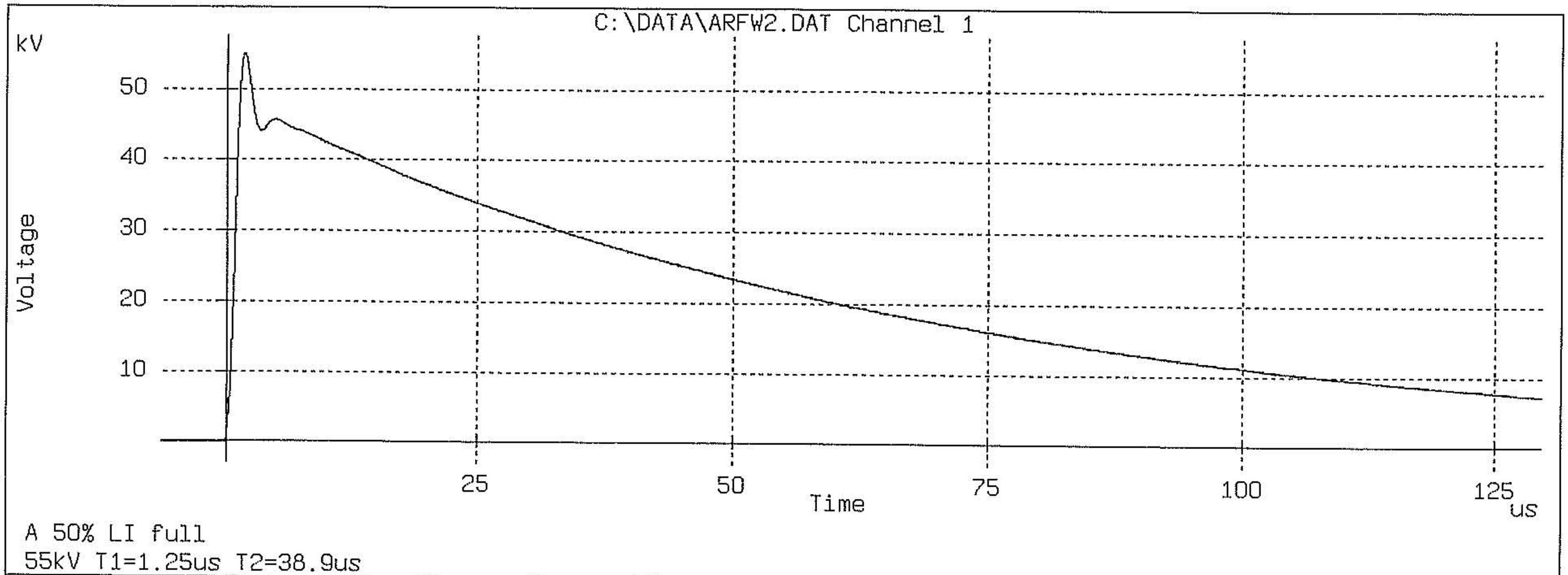
B 100% LI tail chopped
121kV -28.69% T1=1.17us Tc=2.44us

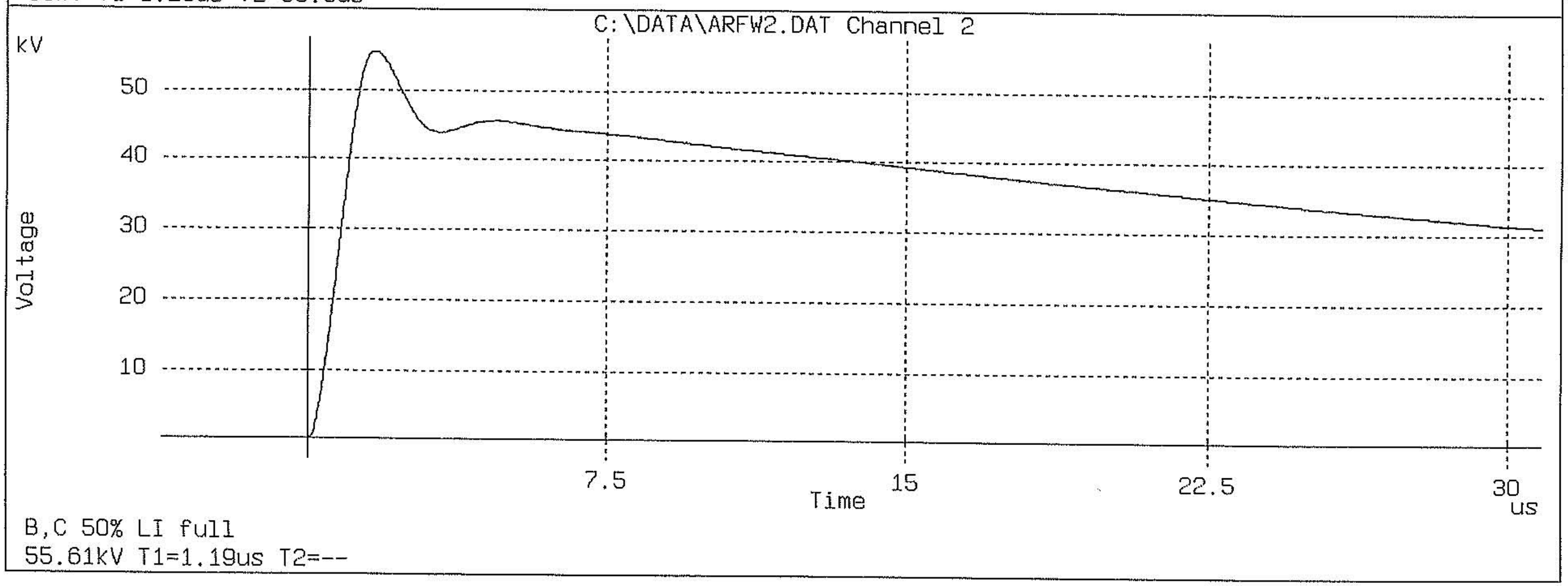


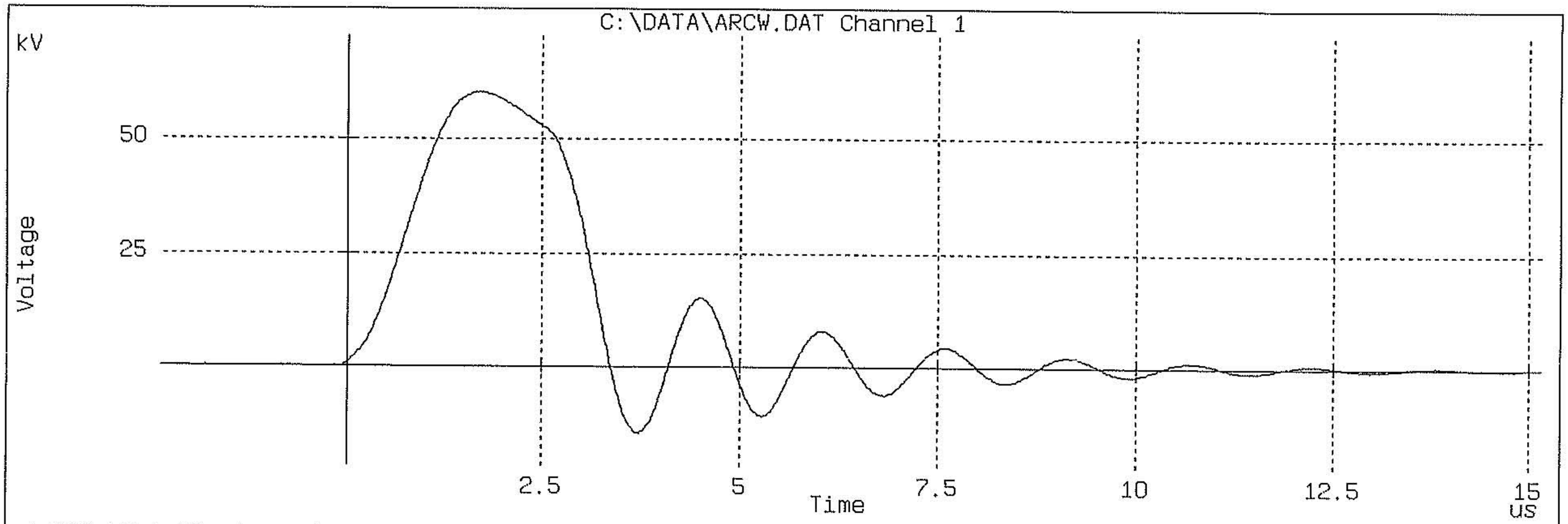
B 100% LI full
110.1kV T1=1.24us T2=39.1us



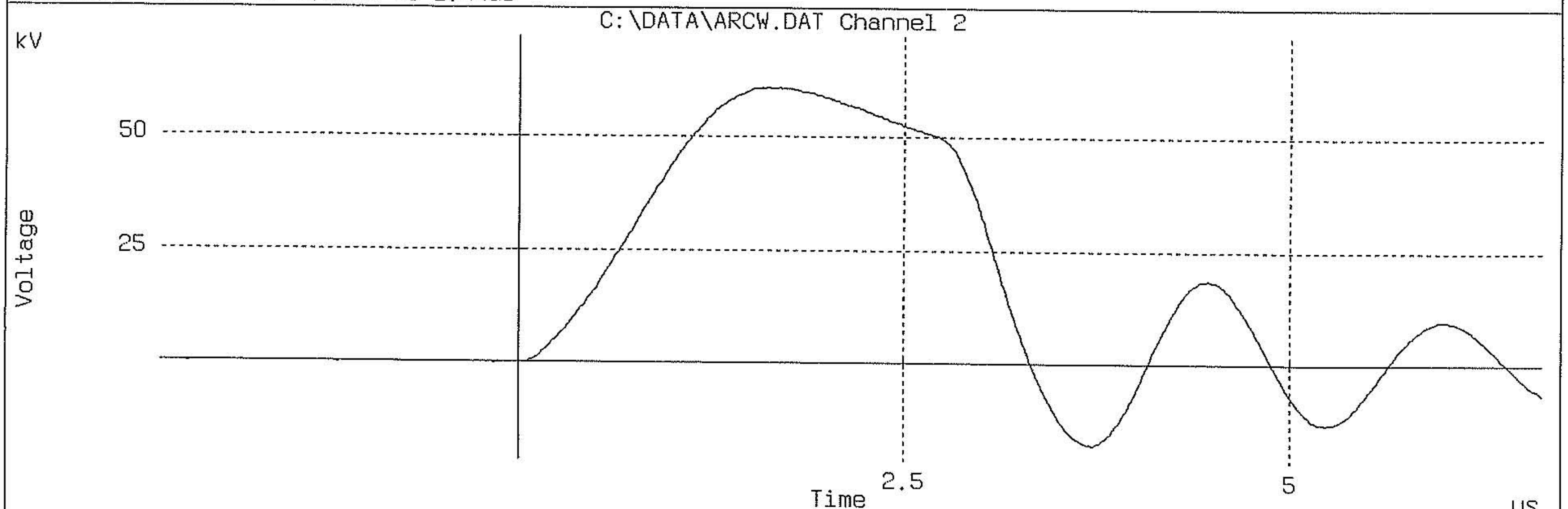
B 100% LI full
111.3kV T1=1.18us T2=--


C:\DATA\ARFW2.DAT Channel 1
kV
Voltage
50
40
30
20
10
25
50
75
100
125
Time
us
A 50% LI full
55kV T1=1.25us T2=38.9us

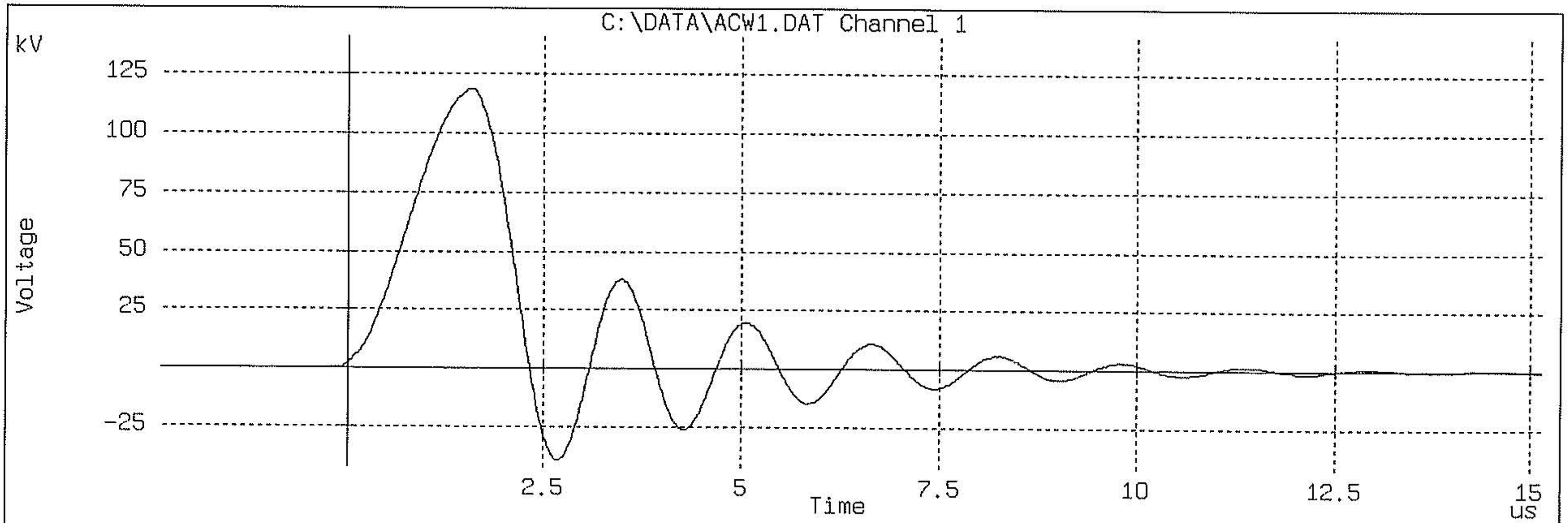

C:\DATA\ARFW2.DAT Channel 2
kV
Voltage
50
40
30
20
10
7.5
15
22.5
30
Time
us
B,C 50% LI full
55.61kV T1=1.19us T2=--



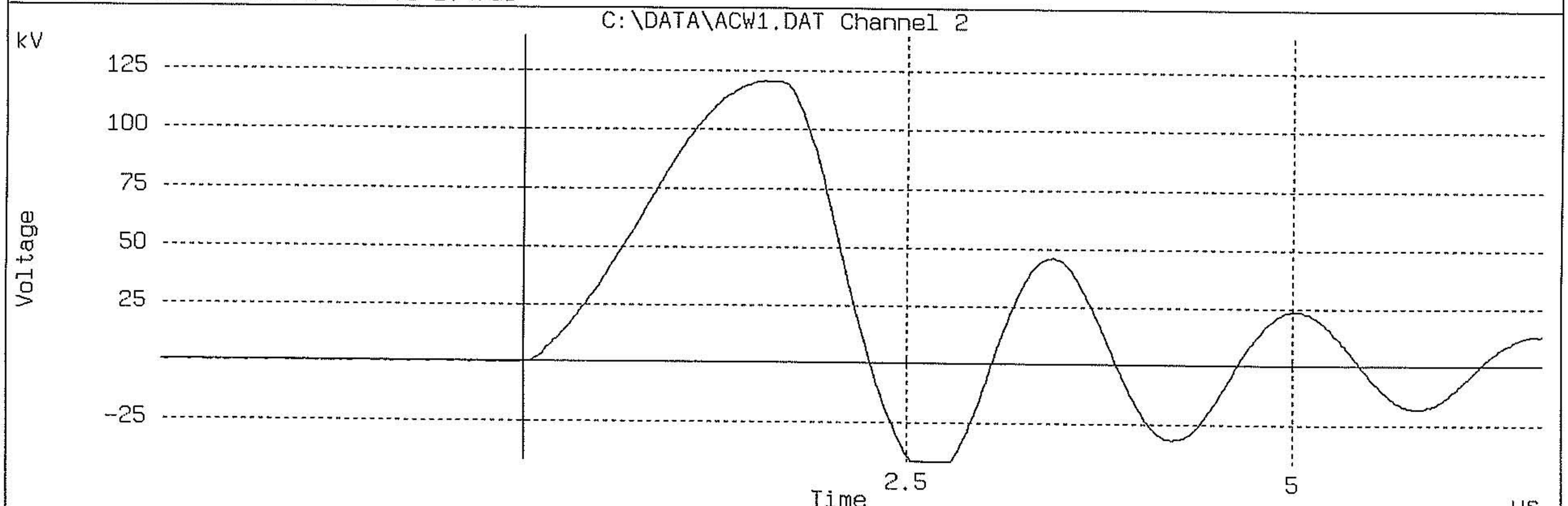
A 50% LI tail chopped
60.06kV -24.04% T1=1.25us Tc=2.44us



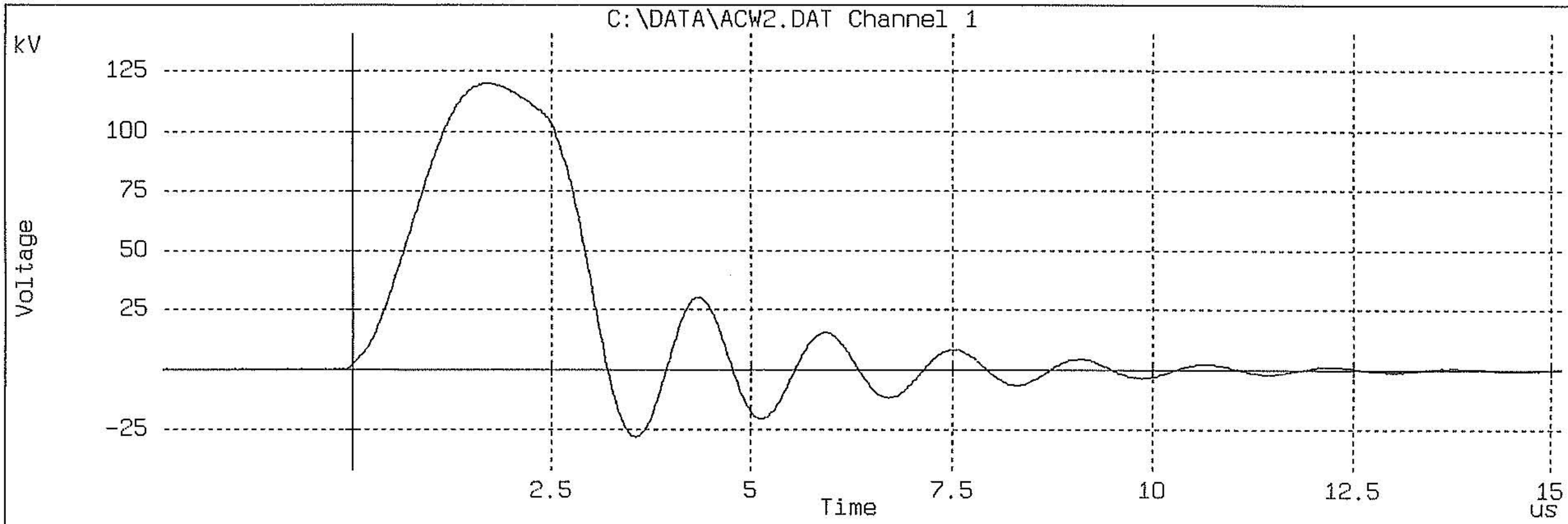
B,C 50% LI tail chopped
60.55kV -29.54% T1=1.18us Tc=2.55us



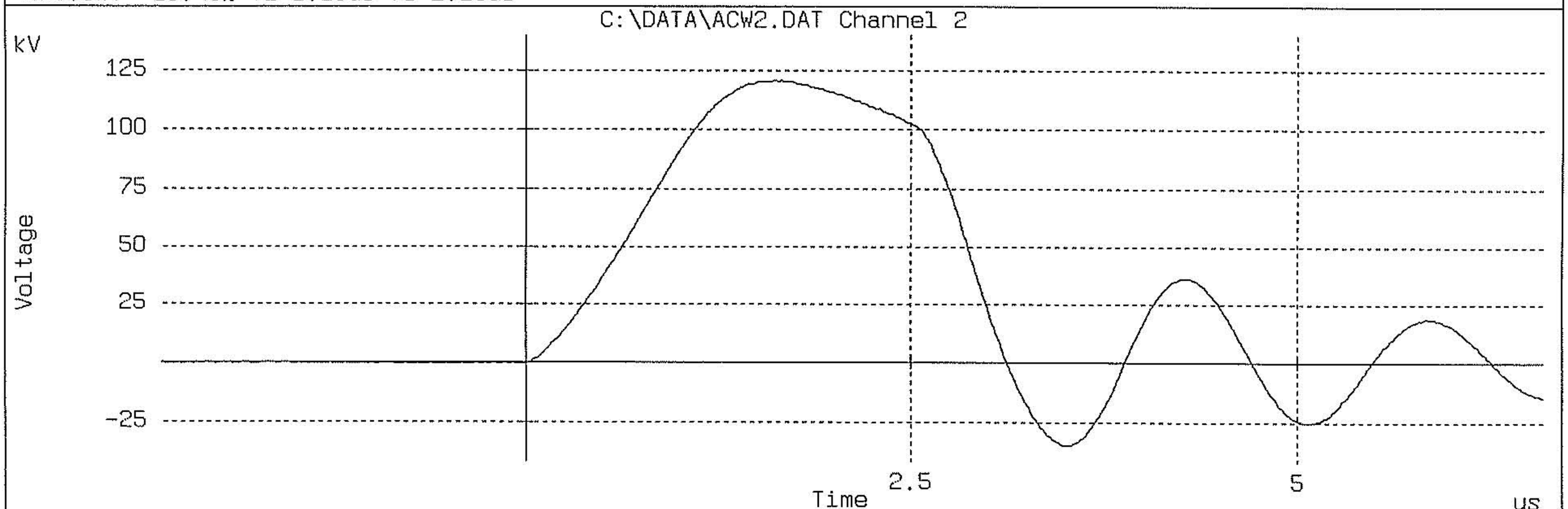
A 100% LI tail chopped
118.3kV -32.78% T1=1.23us Tc=1.47us



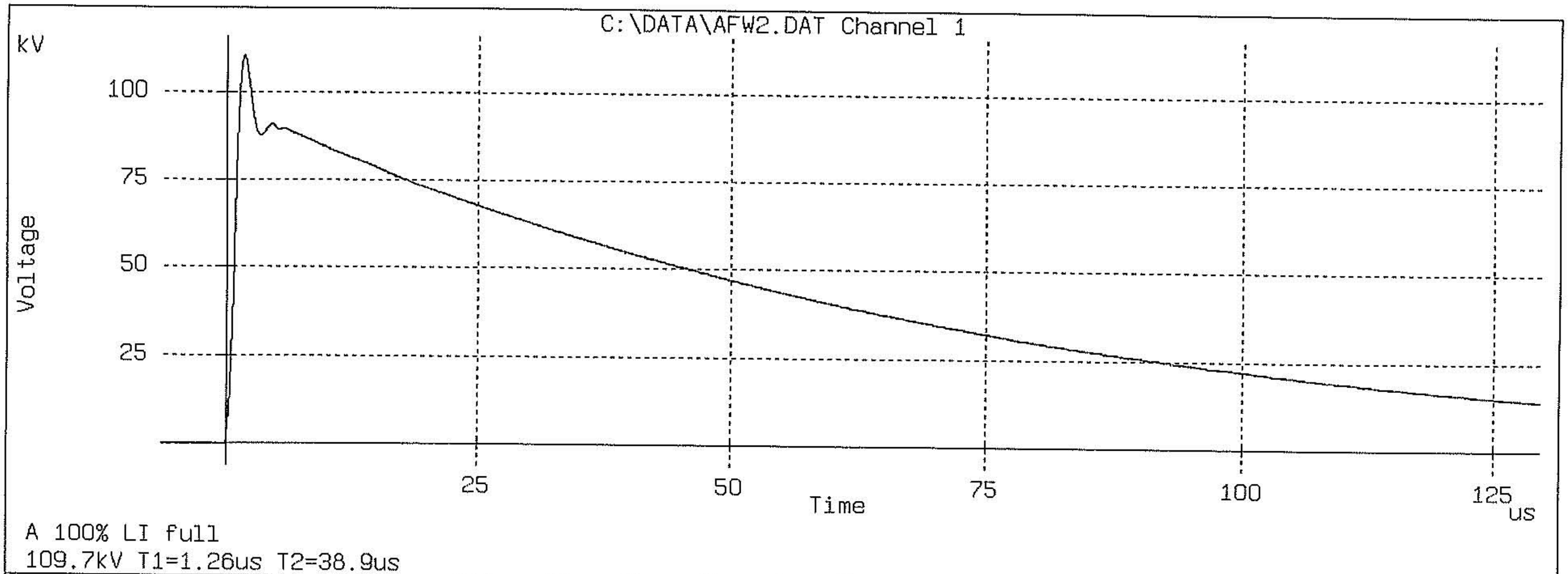
B,C 100% LI tail chopped
120.6kV -34.71% T1=1.19us Tc=1.55us Underflow

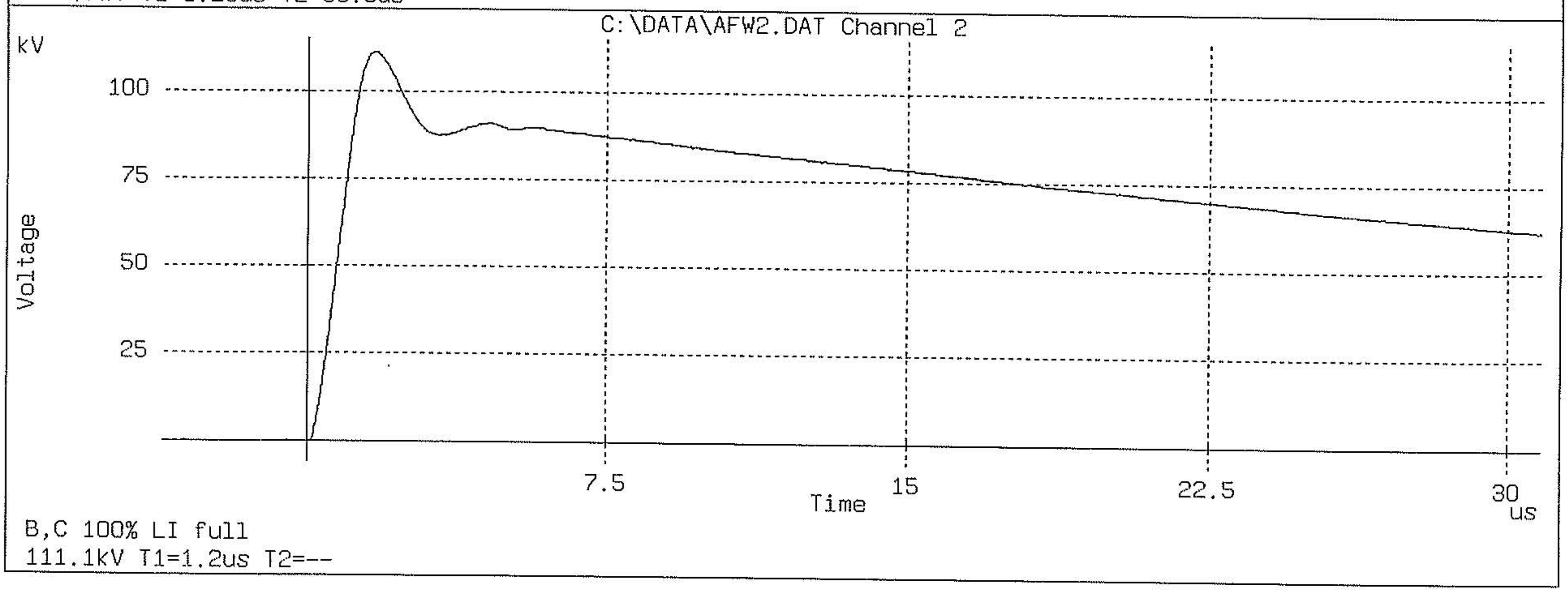


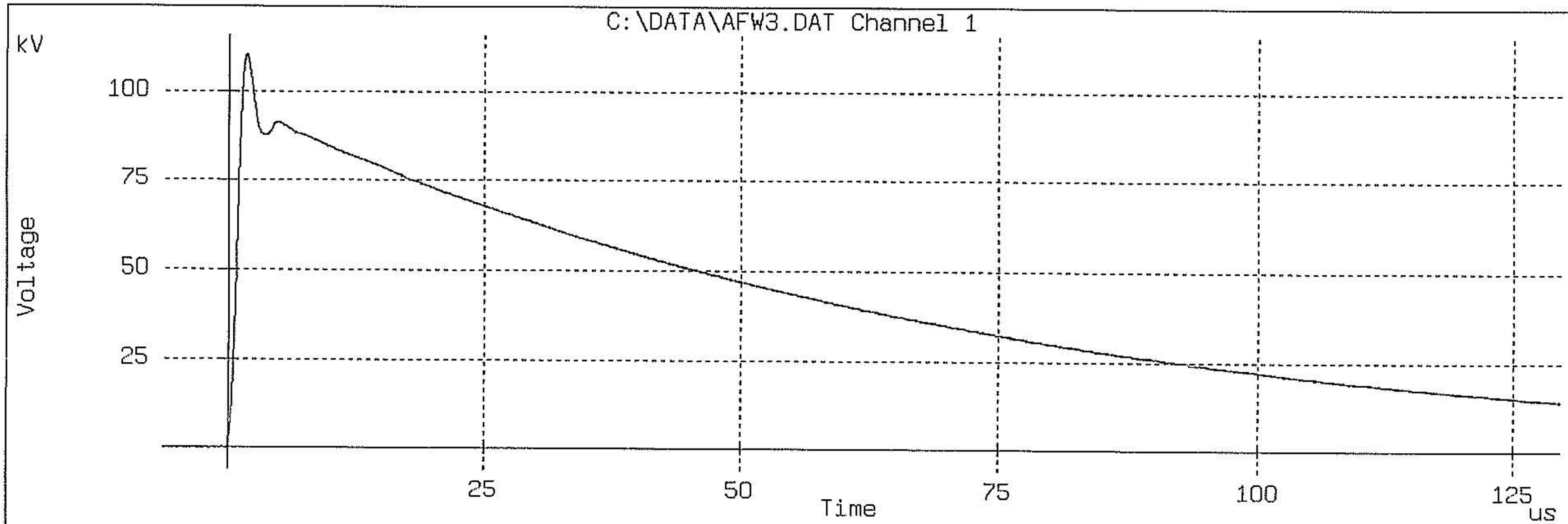
A 100% LI tail chopped
119.5kV -23.48% T1=1.25us Tc=2.25us



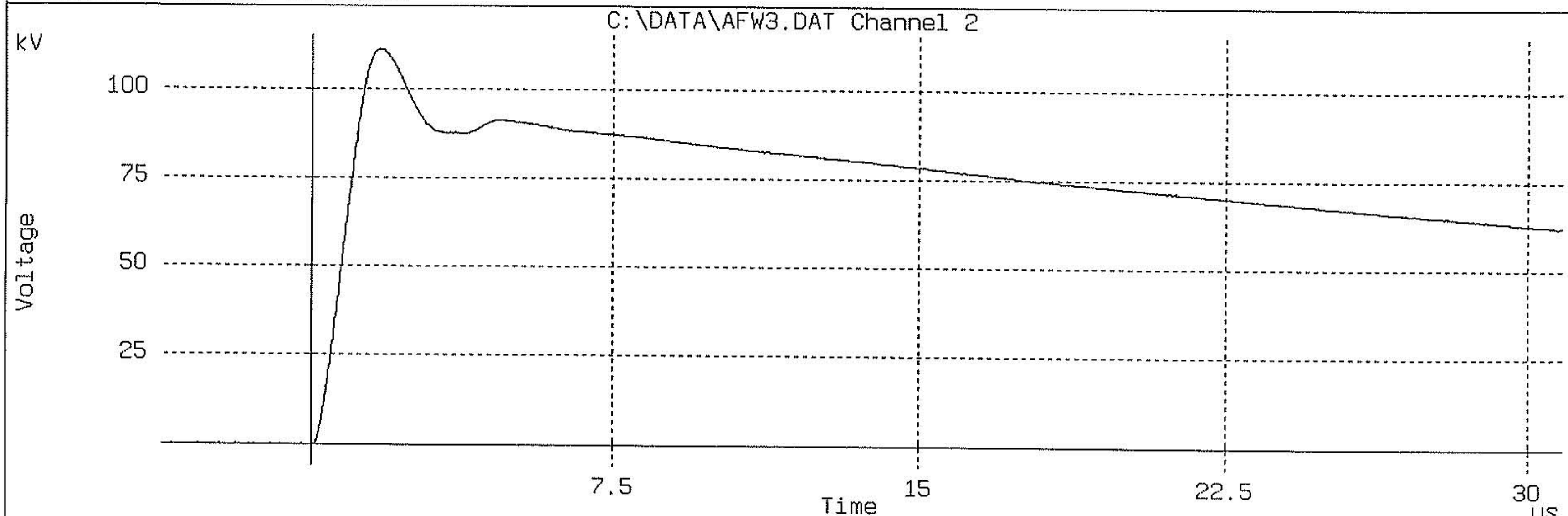
B,C 100% LI tail chopped
120.6kV -28.93% T1=1.2us Tc=2.35us


C:\DATA\AFW2.DAT Channel 1
kV
Voltage
100
75
50
25
25
50
75
100
125
us
Time
A 100% LI full
109.7kV T1=1.26us T2=38.9us

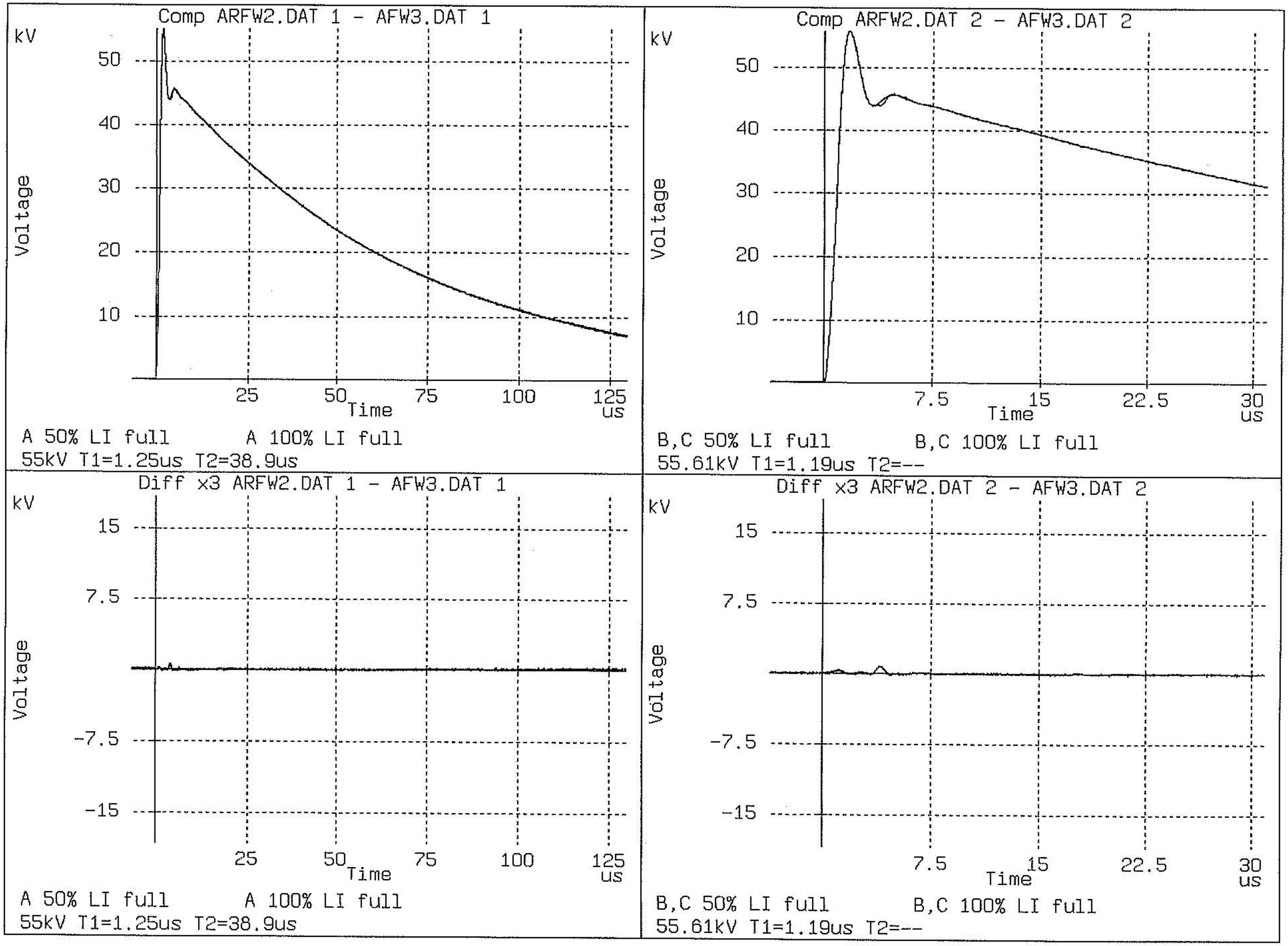

C:\DATA\AFW2.DAT Channel 2
kV
Voltage
100
75
50
25
7.5
15
22.5
30
us
Time
B,C 100% LI full
111.1kV T1=1.2us T2=--



A 100% LI full
109.9kV T1=1.26us T2=38.8us



B,C 100% LI full
111.1kV T1=1.2us T2=--


Comp ARFW2.DAT 1 - AFW3.DAT 1
kV
Voltage
50
40
30
20
10
25
50
75
100
125
us
Time
A 50% LI full
A 100% LI full
55kV T1=1.25us T2=38.9us
Comp ARFW2.DAT 2 - AFW3.DAT 2
kV
Voltage
50
40
30
20
10
7.5
15
22.5
30
us
Time
B,C 50% LI full
B,C 100% LI full
55.61kV T1=1.19us T2=--
Diff x3 ARFW2.DAT 1 - AFW3.DAT 1
kV
Voltage
15
7.5
-7.5
-15
25
50
75
100
125
us
Time
A 50% LI full
A 100% LI full
55kV T1=1.25us T2=38.9us
Diff x3 ARFW2.DAT 2 - AFW3.DAT 2
kV
Voltage
15
7.5
-7.5
-15
7.5
15
22.5
30
us
Time
B,C 50% LI full
B,C 100% LI full
55.61kV T1=1.19us T2=--

APPENDIX G:
Zenergy Power HTS FCL Operation Manual

Fault Current Limiter Operation Manual

June 2011

ZENERGY POWER

www.zenergypower.com

Operation Manual

Reporting Entity:	Zenergy Power Inc. 379 Oyster Point Boulevard, Suite 1, South San Francisco, CA 94080 USA		
Responsible Person:	William Schram		
Project Name:	SCE Avanti Fault Current Limiter		
Document Title:	SCE Avanti Fault Current Limiter Operation Manual		
Document Ref. No.:	ZP/02-2009-04-06		
Date of issue:	06/04/2009		
Client(s):			
Author(s):	William Schram	Approved:	
Distribution:	Southern California Edison		

Summary

This manual is intended to provide instructions for setup, startup, shutdown and routine maintenance of the Zenergy Power Inc. Fault Current Limiter.

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List of Revision

Revision	Date	Action	Modified Page
1	06/04/09	Released	

Contents

1 Applicability

This manual is intended to provide instructions for setup and shutdown of the Zenergy Power Inc. Fault Current Limiter. Also provided are the maintenance intervals for components and a spare parts list.

2 Acronyms

FCL Fault Current Limiter

HTS High Temperature Superconductor

3 Description of the HTS Fault Current Limiter

Figure 1 depicts the fundamental principle of the HTS Fault Current Limiter. During normal operation, a single HTS coil provides the DC bias to maintain a saturated core condition in the two cores of every phase of the FCL.

Notice that for a three phase configuration with the cores arranged in the spider arrangement shown in figure 2, six cores limbs pass through the encapsulated cryostat containing the DC coil and a similar number of external core limbs (two per phase) close the magnetic circuit.

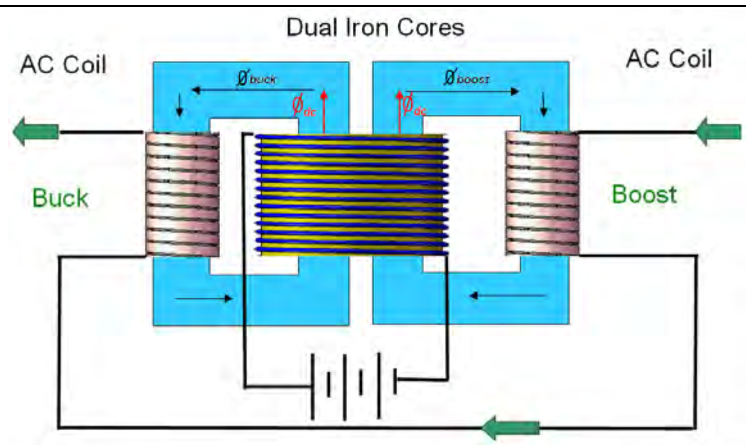

Figure 1: Dual Iron Cores Saturated by one HTS DC coil in a single phase FCL configuration

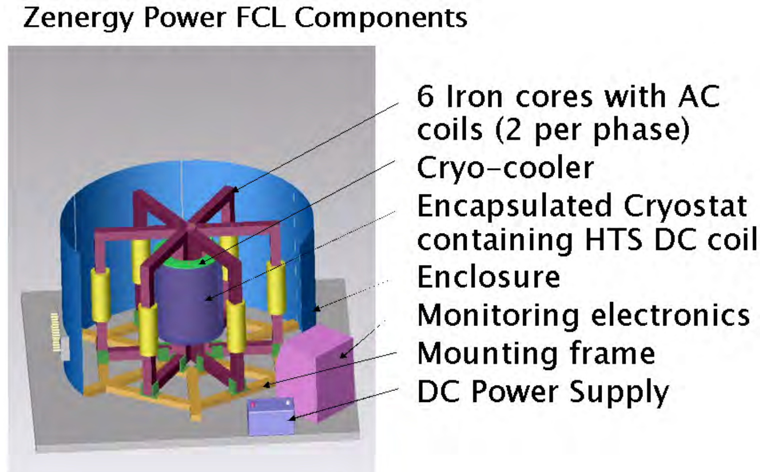

Figure 2: CEC-Avanti Three Phase Spider Configuration FCL

Under normal operating conditions, the "working region" of the FCL on the B-H curve is as shown in figure 3. AC current boosts the magnetic field in one the cores and bucks it on the other. The inductance of the coil is proportional to dB/dH. Therefore in a simple way we can think of a low AC coil inductance when the core is driven into deep saturation and of a high AC coil inductance when the core is taken out of saturation.

Therefore, the ZP FCL shows fundamentally low insertion impedance under normal operating conditions while it will attain high inductance values under a fault as the current swings between positive and negative peak values. This will drive the AC coils through high inductance regions as they transit over high slope regions on the B-H plane. This is illustrated in figure 4 where the magnetic flux is plotted versus current.

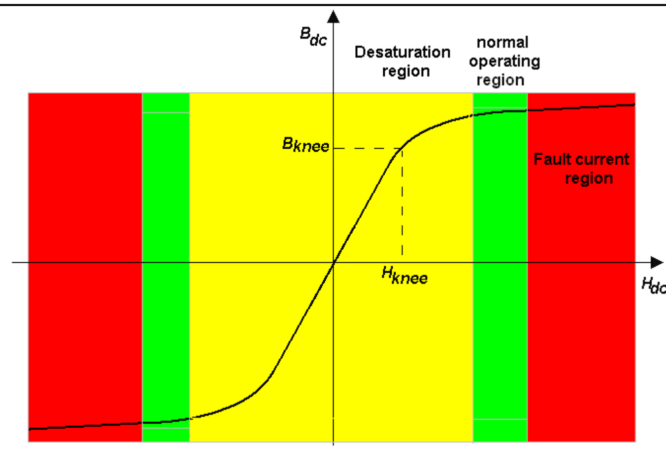

Figure 3: Operating region of the saturable-core type FCL

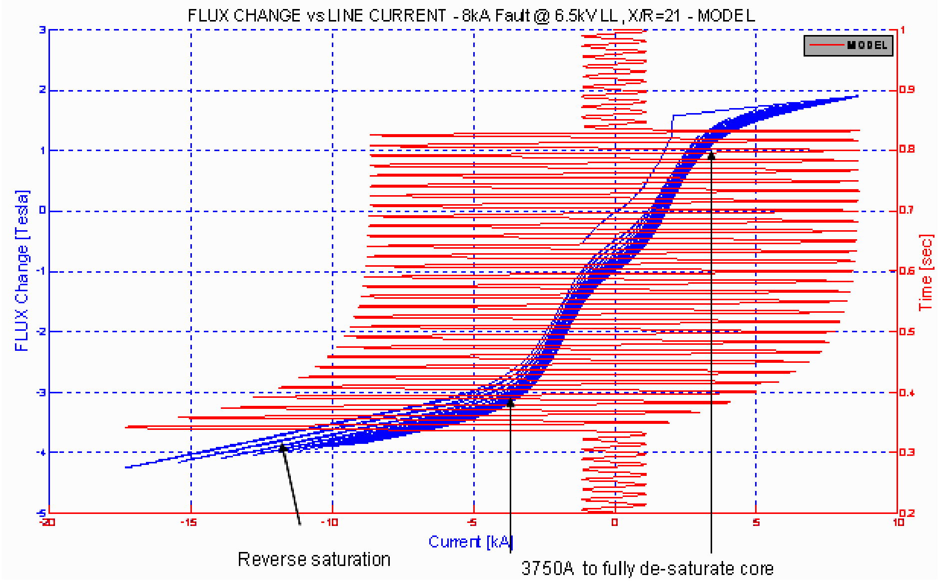

Figure 4: Flux versus current under a fault on the ZP FCL

4 Setup Auxiliary Power and Communications

4.1 Auxiliary Power

The auxiliary power cable is fed through the bottom of the enclosure base plate into cutout box containing the terminal blocks, as shown in Figures 5 and 6.

Figure 5: Auxiliary Power Cable Feed Through

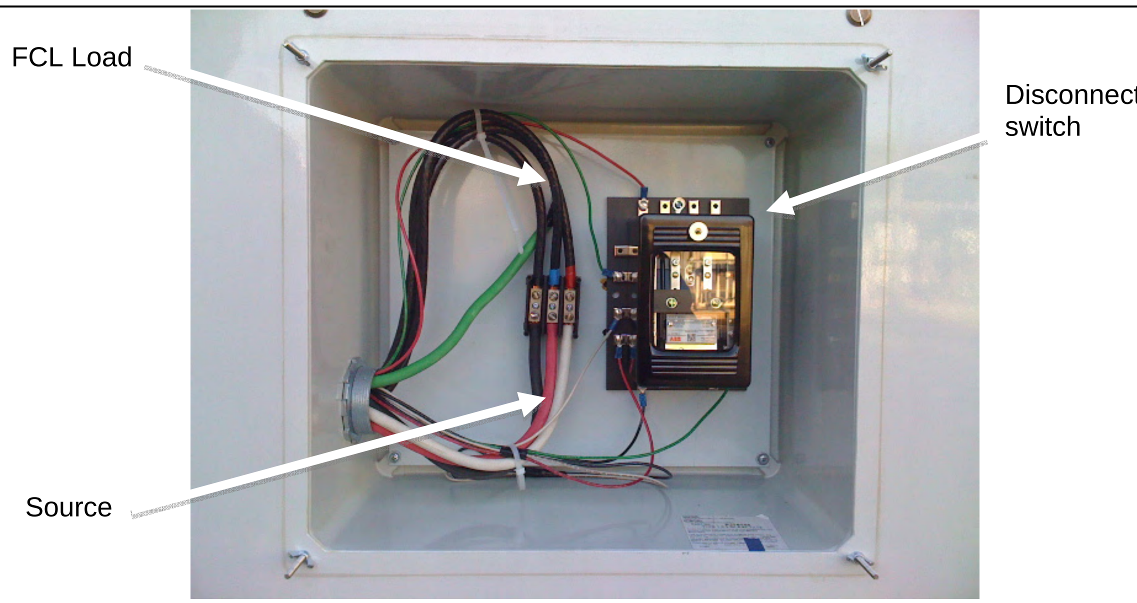

Figure 6: Auxiliary Power Terminal Blocks

Once the auxiliary power is wired as shown above be sure to confirm the phasor rotation is negative. Compressor functionality in the FCL is rotation specific.

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4.2 Fiber Optic Communications Via Modbus

The fiber optic communications to the FCL are transmitted over a single-mode fiber optic cable. This cable is connected inside the electronics cabinet to a Fiber-to-Ethernet converter module, which then connects directly to the programmable automation controller (PAC).

Modbus Connection: Modbus slave set up on IP Address 192.168.140.31, Service Port 502, Address 2.

Modbus Data List:

Measurements	Data Type	Address	Description	Status	Units
FCLBypass	Boolean	100001	True indicates the FCL should be bypassed	OK	T/F
Heartbeat	UInt16	400091	Heartbeat counter that increments by 1 every 200 milliseconds	OK	numerical
Top Cover 1 Temp	Single	F400001	Signal from Type-K TC on Cryostat Lid	OK	Kelvin
Top Cover 2 Temp	Single	F400003	"	OK	Kelvin
Ambient Temp	Single	F400005	Unconnected signal	N/A	N/A
Digital Input Lines	UInt16	400092	Collection of digital inputs to the PAC (listed below without address)	OK	NIL
Compressor 1 Relay Status	Boolean	LSB0	Relay controlling power to compressor 1	OK	T/F
Compressor 2 Relay Status	Boolean	LSB1	Relay controlling power to compressor 2	OK	T/F
PS2 Relay Status	Boolean	LSB2	Relay putting PS1 in circuit	OK	T/F
PS1 Relay Status	Boolean	LSB3	Relay putting PS2 in circuit	OK	T/F
UPS Low Battery	Boolean	LSB4	UPS status	OK	T/F
UPS On Battery	Boolean	LSB5	UPS status	OK	T/F
UPS Fault Battery	Boolean	LSB6	UPS status	OK	T/F
Backup Charger Status	Boolean	LSB7	Auto-actuated relay indicating presence of 120 VAC wall-power supply	OK	T/F
HTS Backup Enable Relay Status	Boolean	LSB8	Relay putting HTS Backup battery in circuit	OK	T/F
PS2 Manual Switch Status	Boolean	LSB9	Status of switch to manually control PS2 contactor	OK	T/F
PS1 Manual Switch Status	Boolean	LSB10	Status of switch to manually control PS1 contactor	OK	T/F
FCL Bypass Relay Status	Boolean	LSB11	Unwired placeholder for FCL Bypass switch status readback	N/A	N/A
Top Cover Heater Relay Status	Boolean	LSB12	Status of Top Cover heater power contactor	OK	T/F
HTS Current	Single	F400021	Current through DC Coil	OK	Amps
HTS Voltage	Single	F400023	Voltage across DC Coil	OK	Volts
Total DC Current	Single	F400025	Current through DC Coil and dump resistor	OK	Amps
VTap 1	Single	F400027	Voltage diffrential between coil tap 1 and 9	OK	Volt
VTap 2	Single	F400029	Voltage diffrential between coil tap 2 and 9	OK	Volt
VTap 3	Single	F400031	"	OK	Volt
VTap 4	Single	F400033	"	OK	Volt
VTap 5	Single	F400035	"	OK	Volt

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VTap 6	Single	F400037	"	OK	Volt
VTap 7	Single	F400039	"	OK	Volt
VTap 8	Single	F400041	"	OK	Volt
VTap Ref	Single	F400043	Absolute voltage at tap 9	N/A	N/A
LN2 Pressure	Single	F400007	Nitrogen Pressure inside cryostat	OK	Torr
Vacuum Pressure	Single	F400009	Vacuum pressure inside insulating walls of cryostat	N/A	N/A
Battery Charging Current	Single	F400011	Current charging backup battery	OK	Amps
LN2 Level	Single	F400013	Level of liquid nitrogen inside cryostat	OK	cm
Phase A Voltage	Single	F400045		OK	V rms
Phase B Voltage	Single	F400047		OK	V rms
Phase C Voltage	Single	F400049		OK	V rms
Phase A Current	Single	F400051		OK	A rms
Phase B Current	Single	F400053		OK	A rms
Phase C Current	Single	F400055		OK	A rms
UPS Voltage	Single	F400015	Voltage supplied by UPS to PAC and some meters	OK	Volt
Coil Top Temperature	Single	F400057	HTS Coil Temperature at top	OK	Kelvin
Coil Bottom Temperature	Single	F400059	HTS Coil Temperature at bottom	OK	Kelvin
Coldhead 1 Temperature	Single	F400061	Cryo-cooler 1 temperature (inside cold head)	OK	Kelvin
Coldhead 2 Temperature	Single	F400063	Cryo-cooler 2 temperature (inside cold head)	OK	Kelvin
PS1 Voltage	Single	F400065	Voltage reading from PS1	OK	Volt
PS1 Current	Single	F400067	Current reading from PS1	OK	Amp
PS2 Voltage	Single	F400069	Voltage reading from PS2	OK	Volt
PS2 Current	Single	F400071	Current reading from PS2	OK	Amp
Red Alarm Status	UInt16	400094	Red Alarm Status bits (give reason for bypass and shutdown)		
UPS Low Battery		LSB0	UPS operating on battery and low battery indicator is on	OK	T/F
UPS Fault		LSB1	UPS Faults occur (unused)	N/A	
UPS Voltage		LSB2	UPS voltage supply is out of bounds	OK	T/F
HTS Temp		LSB3	HTS Coil temperature rises above critical level	OK	T/F
VTap Quench		LSB4	HTS Coil voltage differentials above critical level	OK	T/F
HTS Voltage		LSB5	HTS Coil voltage rises above critical level	OK	T/F
HTS Current		LSB6	HTS Coil current drops below critical level	OK	T/F
HTS Backup Present		LSB7	HTS Backup battery drops out of circuit	OK	T/F
HTS Backup Duration		LSB8	HTS Coil running on battery backup longer than configurable duration	N/A	
240 VAC Supplied		LSB9	Wall power not available	OK	T/F
PT Drop		LSB10	Voltage drop across FCL above limit (unused)	N/A	
User Shutdown		LSB11	User initiated shutdown	OK	T/F

Key:

Single is a 32-bit floating point number

UInt16 is 16-bit unsigned integer

The Uint16 is used in two places to hold 16 bits of digital status data, but for implementation efficiency reasons it is mapped to a UInt memory space in modbus

5 Cool Down of HTS Magnet in Cryostat

The cryostat requires approximately 500 liters of gaseous and liquid nitrogen to cool down and fill the vessel to its operating level. Nitrogen dewars (liquid nitrogen containers) can be procured from Praxair, Air Products, or Airgas. The industry standard is the 200-liter Dewar illustrated in Figure 6; the cryostat requires three of these to fill.

Figure 7: Liquid Nitrogen Dewars

To fill the cryostat, remove the ISO KF 25 clamp and cap from the KF 25 flange located above the cryostat vacuum valve and adjacent to the recondenser basin. In Image of the KF 25 flange is shown below in Figure 8.

Figure 8: Liquid Nitrogen Fill Port

Connect the appropriate fill hose and purge the vessel with cold gaseous nitrogen for two hours. Then switch to liquid nitrogen and begin filling. The vessel should cool at a rate no greater than 50 Kelvin per hour; this information can be acquired from the bottom coil temperature sensor readout on the Lab View User Interface.

Once the bottom coil temperature reads 100 Kelvin the cool-down rate can be neglected and the vessel can be filled as fast as the liquid nitrogen can be delivered. The stop point for filling is 83.9 centimeters on the nitrogen level readout; this value is 100 percent of the calibration range above this height no sensing is available. When the fill height is achieved, ensure all flanges on the lid of the cryostat are tightly sealed.

6 Startup Sequence

Begin by turning on all switches of the electronics cabinet, as shown in Figure 9.

Figure 9: Power Switches in ON Position

Currently the controller receives commands from a remote terminal operated by Zenergy Power for completion of the startup sequence. This is a safety precaution to ensure the superconducting magnet is not energized without a Zenergy Power staff member present.

A Zenergy representative will then turn on Compressor One. This is accomplished by closing the switch for Compressor One located on the LabVIEW user interface. A relay should be heard closing and then the compressor will turn on. Next the HTS magnet will be manually ramped to a 100 amp bias on the LabVIEW user interface. This will conclude the Startup Sequence for the fault current limiter. Now the FCL can be switched into the circuit.

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7 Shutdown Sequence

In the event of a decommissioning or auxiliary power failure, the fault current limiter will initiate the shut down procedure. This implies a shut down can be initiated simply by opening the auxiliary power circuit. First the disconnect relay will trip to initiate the automated disconnect of the FCL and an alert will be sent via the modbus communication indicating the FCL is shutting down. Next the battery backup will ramp down the superconductor coil. Once confirmation has been made that ramp down of the magnet has completed, this is done by visually confirming the HTS Coil Amperage meter is at zero amps on the display window, turn all switches on the electronics cabinet off as shown in Figure 10 below.

Figure 10: Power Switches in OFF Position

8 Maintenance

Maintenance is to be performed by Zenergy Power staff and will require the participation and assistance of SCE in scheduling a bypass of the FCL.

8.1 Maintenance Schedule

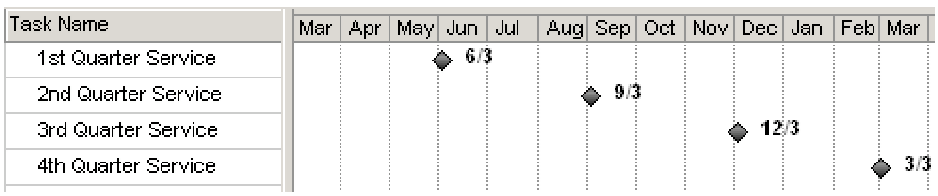

Figure 11: Maintenance Schedule, Assuming a March 3rd Commissioning Date

<u>HVAC System (Pages 15-18 of the Liebert Intelecool2 User Manual)</u>

- Filter: Replace quarterly.
- Blower: Check quarterly for debris, the shaft should rotate freely.
- Economizer: Check quarterly for debris.
- Refrigeration: Check quarterly for signs of wear and proper operation.

<u>Cryomech Compressor and Cold Head Assemblies:</u>

- Compressor Filter: Every quarter or 2000 hours of operation replace compressor filter.
- Cold Head: After four quarters or 10,000 hours of operation the piston assembly in the cold head should be inspected by a Cryomech trained service representative.
- After eight quarters of operation or 20,000 hours a complete overhaul of the piston assembly is necessary. The cold head should be extracted from the roof of the FCL enclosure and shipped to Cryomech for service. In advance of this service a replacement cold-head assembly should be procured.

<u>Lambda Power Supplies:</u>

Power Electronics in the power supply are rated for a four-year operating life or sixteen quarters. After the power supply has been in service for four years replace the units to ensure no discontinuity in service.

8.2 Maintenance Contacts

Primary Contact

Company:	Zenergy Power
Office Phone (8-5):	650-615-5720
Address:	379 Oyster Point Blvd, Suite 1
	South San Francisco
Emergency Contact:	Franco Moriconi
Emergency Phone:	510-334-9534

Service Contacts

Company:	Liebert Corporation, Associates of San Francisco
Tech Support:	1-800-543-2778
Address:	1050 Dearborn Drive
	P.O. Box 29186
	Columbus, OH. 43229

Company:	Cryomech, Inc.
Office:	315-455-2555
Address:	113 Falso Drive
	Syracuse, NY. 13211

Company:	Lambda Americas, Inc.
Office:	732-922-9300
Address:	405 Essex Road
	Neptune, NJ. 07753

9 Spare Parts List

1. Air filter for the Cryomech compressor, two units
2. Air filter for HVAC, one unit per
3. 5 amp fuse
4. 10 amp fuse
5. 20 amp fuse
6. Sidewalk Bolts, 0.25 inch DIA by 2 inch
7. NI cFP-2200 National Instruments Controller
8. Replacement cold-head, Modified AL-300
9. Potential transducers spare 15kV fuse
10. 24Volt Relay
11. 120 volt Relay

10 Bill of Materials

Item number	Part number	Description	Default/QTY.
1	CEC-08-0000	CEC-FCL-092408	1
2	CEC-08-0001	Reactor Assembly	1
3	CEC-08-0002	DC Cables	4
4	CEC-08-0003	AUX Power Box	1
5	CEC-08-0004	Baseplate Assembly	1
6	CEC-08-0005	AC Current Transducer Model CTDZ	3
7	CEC-08-0006	Pie Core Assembly	6
8	CEC-08-0007	900 Amp Bushing 052008	6
9	CEC-08-0008	Deadbreak stand	6
10	CEC-08-0009	Step Enclosure	1
11	CEC-08-0010	Electronics Assembly	1
12	CEC-08-00101	Compressor	2
13	CEC-08-00102	Enclosure Power Supply	1
14	CEC-08-00103	AC Unit	1
15	CEC-08-00104	U-channel	2
16	CEC-08-00105	Lapp Insulator	4
17	CEC-08-0011	02-1002-2002-05 AC Coil 050708	6
18	CEC-08-0012	Enclosure 051208	1
19	CEC-08-0013	Busbar Shorter	3
20	CEC-08-0014	Thermalsyphon Side 041508	1
21	CEC-08-0015	Cryostat	1
22	CEC-08-0016	He Hose	2
23	CEC-08-0017	HVAC System	1

11 References

"Liebert InteleCool 2: User Manual – Outdoor Wall-Mount Air Conditioner, 1.5-5 Tons, 50-60 Hz", HVAC Manual

"Cryomech AL300 Cryogenic Refrigerator – Installation, Operation, Routine Maintenance Manual", Cryo-Refrigeration Manual

"Fieldpoint Operating Instructions and Specifications –

CFP-2200/2210/2220", Controller Manual from National Instruments

"Material Safety Data Sheet – Liquid Nitrogen", Air Products.

MSDS number 30000000010

APPENDIX H:
Zenergy Power HTS FCL Cryostat Evacuation and Moisture Removal Procedure

Engineering Report

Cryostat Evacuation and Moisture Removal Process

June 2011

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Engineering Report

Status (Final or Draft):	DRAFT		
Reporting Entity:	Zenergy Power Inc. 379 Oyster Point Boulevard, Suite 1, South San Francisco, CA 94080 USA		
Responsible Person:	Amandeep Singh		
Project Name:	SCE Avanti Fault Current Limiter		
Document Title:	Cryostat Evacuation and Moisture Removal Process		
Document Ref. No.:	ZP/ER-2009-09A		
Date of issue:	MM/DD/YYYY		
Client(s):	Zenergy USA Internal		
Author(s):	Erica Klett		
Distribution:	Internal	Approved:	F. Moriconi

Executive Summary

The FCL at Shandin substation required Liquid Nitrogen fill. This report describes the process for evaporating the remaining LN2, removing moisture and vacuuming system to acceptable level for the Cryomech Cold-Head test.

The LN2 chamber was successfully evacuated, to a final vacuum level of ~2mTorr.

List of Revisions

Revision	Date	Action	Modified Page
A	MM/DD/YY	Initial Release	

Contents

1 Objective

In order to service and refill the Fault Current Limiter Liquid Nitrogen chamber, the remaining liquid must be removed and all the moisture evaporated. Heat, warm nitrogen gas and vacuum pumping can aid the evaporation process and remove the moisture.

2 Acronyms

FCL	Fault Current Limiter
LN2	Liquid Nitrogen
AMI	American Magnetics, Inc.
HTS	High Temperature Superconductor
PPE	Personal Protective Equipment

3 Process

1. Evaporate LN2
2. Remove Moisture
3. Achieve Ambient Temperature
4. Vacuum Pump System

4 Initial Conditions

The FCL had about 25cm of remaining LN2 in the vessel.
The Liquid Nitrogen chamber has a heater coil installed to heat the internal chamber and assist in evaporating the LN2. However, it was discovered after inspection, that the electrical connection for the LN2 heaters was disconnected from the input power. In addition, it appeared that the wires were too short to reach the connector to attach a power source. Before we could continue, modification of the wire connections was required to connect power to heat the coils.

5 Required Tools, Test Equipment and Drawings

5.1 Tools and Equipment

- Screwdriver
- (2) 10 foot pieces of electrical wire
- (4) Alligator Clips
- Insulated material for wire repair
- Electrical tape
- Heat shrink tubing
- Heat gun
- Space heater
- Vacuum sealed cryogenic hose
- KF clamp
- Compressed Nitrogen gas
- Hose for Nitrogen bottle

5.2 Test Equipment

- Fluke Clamp Meter

- Fluke Multimeter

5.3 Drawings or Schematics

Electrical Schematic for Heater Circuit

6 Hazards, PPE and Equipment Protection

6.1 Hazards

- Regardless of protective equipment, never touch live electrical parts.
- Compressed Nitrogen gas is a material considered hazardous by the OSHA Hazard Communications Standard (29 CFR 1910.1200). Effects of a Single (Acute) Overexposure:
  - Inhalation. Asphyxiant. Effects are due to lack of oxygen. Moderate concentrations may cause headache, drowsiness, dizziness, excitation, excess salivation, vomiting, and unconsciousness. Lack of oxygen can kill.

6.2 Personal Protective Equipment

When dealing with the compressed Nitrogen, the following PPE should be used:

- Skin Protection: Wear work gloves when handling cylinders and metatarsal shoes for cylinder handling. Select in accordance with OSHA 29 CFR 1910.132 and 1910.133.
- Eye/Face Protection: Wear safety glasses when handling cylinders. Select in accordance with OSHA 29 CFR 1910.133.

6.3 Equipment Protection

Referred to design of heaters to verify electrical limitations and discussed our process with management. It was decided that it was safe for the equipment inside the chamber to be heated for as long as required.

7 Isolation and Shutdown Procedure for LN2 Wire Repair

Removed all power to the plug and heater circuit (already disconnected)

8 Steps to Troubleshoot and Provide Power to LN2 Heaters

1. Reviewed schematic for heaters
2. Heaters are rated for 230V and 190 Ohms, current 1.217 Amps, 280 Watts
3. Measured resistance of internal heaters to confirm proper value per design:
   a. Brown and Blue wires = 190ohms
   b. Brown and Yellow/Green wires = Infinity
   c. Blue and Yellow/Green wires = Infinity
4. Determined that the Brown and Blue wires are connected to the heaters, which is consistent with the available circuit documentation.
5. Very slowly and carefully lifted the outer flange and the feed-through away, to make space for repair. See Figure 1 below.

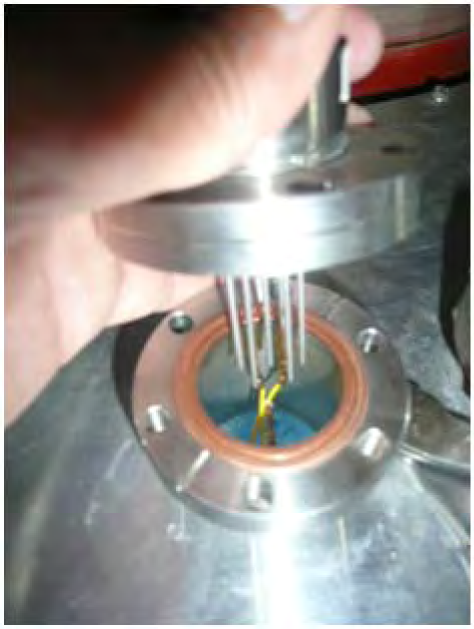


Figure 1: Carefully removed plug to assess repair

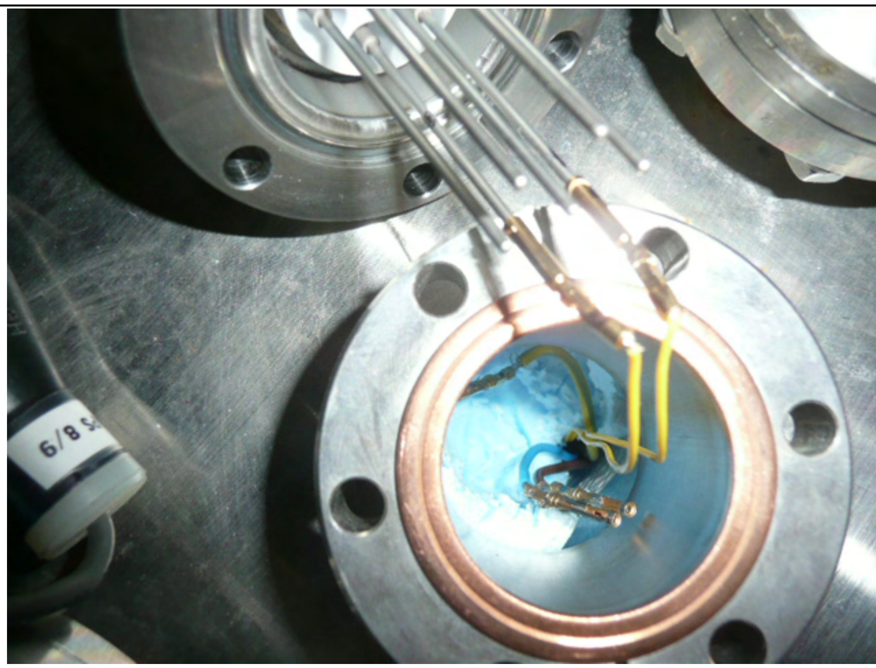


Figure 2: Wires for heaters are disconnected and too short to reach plug

6. Tried pulling out the heater wires with no success.
   a. Made connections locally (right inside the hole) with insulated alligator clips. Figure 2 below shows connection.
   b. Provided insulation between connections for additional safety

Figure 3: Made connection to heaters via alligator clips

7. Applied 238VAC momentarily to energize the heater coil and measured current with a Fluke meter.
   a. Current Measured: 1.20 Amps (consistent with the specifications for the heaters) (See Figure 6)
8. Applied constant 238VAC to energize the heater coil and apply heat to the LN2 chamber.

Figure 4: Checking phase to ground voltage

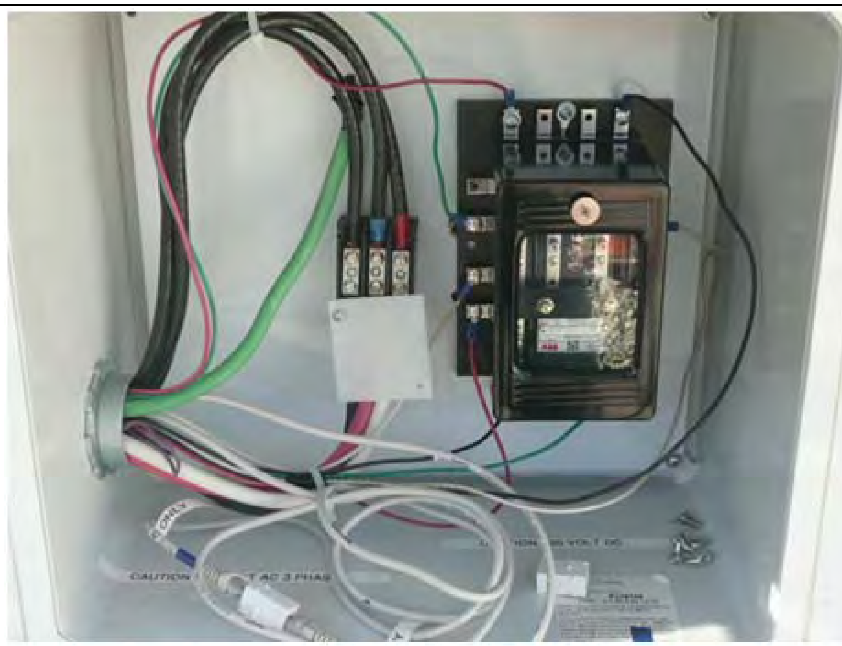


Figure 5: Voltage source used to energize heaters

Figure 6: Clamp meter measuring current across heater circuit, with ~238 Volts applied

9 Liquid Nitrogen evaporation and Moisture Removal Process

1. Applied ~238V to heaters to apply local heat to LN2 chamber.
2. Attached a clamp meter for continuous measurement of heater current.
3. Connected an air source (Heat Gun) to the port of the LN2 chamber to inject air into the space, see Figure 7.
4. Monitored LN2 level on the AMI 186 and FCL monitor. Refer to Figure 8 for plot of data.

Figure 7: Ambient cool air injected into port of LN2 chamber

9.1 LN2 Evaporation Observations:

When the gauges showed that the LN2 level reached zero, we measured the LN2 level with the dipstick. It was discovered that the measured level did not match the gauge reading. After extrapolating the data, we determined that it would take several more hours to completely remove the moisture from the chamber, according to the dipstick measurements. We installed a floor heater in the FCL cabinet, to increase the ambient air temperature that would go into the heat gun attached to the chamber. Figure 9 shows the floor heater.

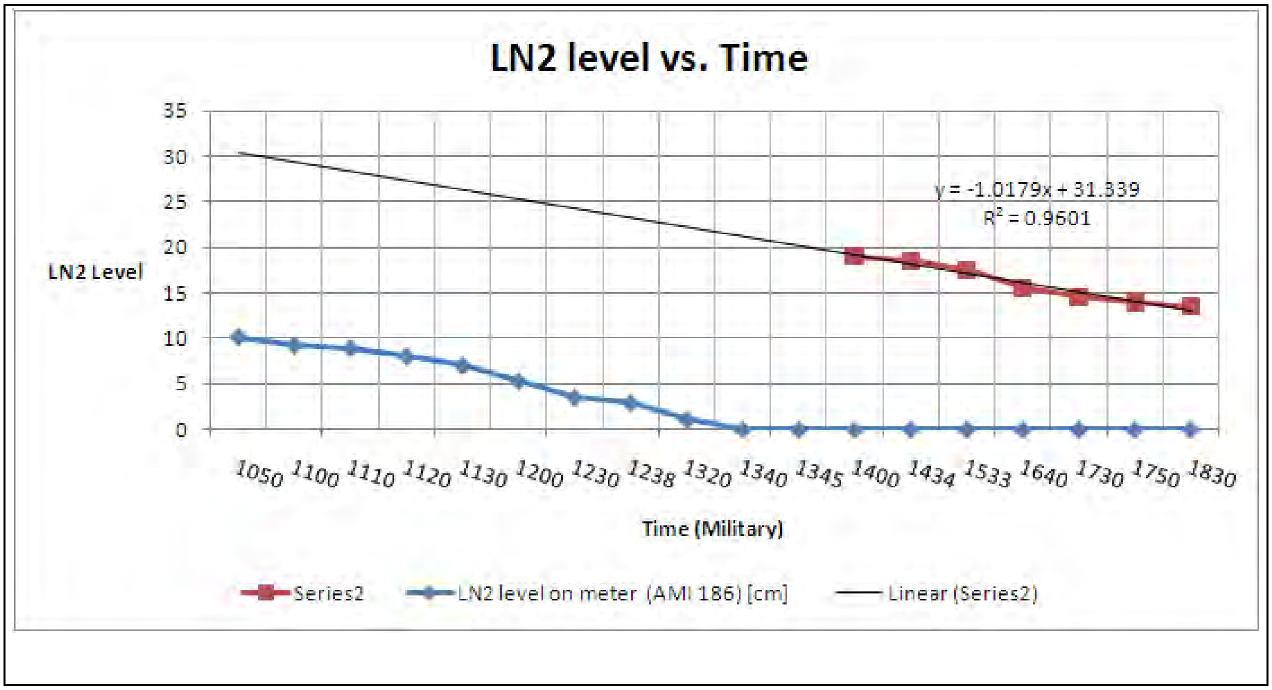


Figure 8: Plot of LN2 level over time, with applied heat

Figure 9: Area heater to safely heat the ambient air for the heat gun

9.2 Evaporation Results

The FCL was left overnight (11/3) in the following configuration:

- Heat gun attached to a fill port (cool temp setting)
- Floor heater placed inside the closed FCL cabinet
- LN2 heater coil energized with 238 Volts

When we returned to the site at 7AM the next day (11/4), we measured the LN2 level with a dipstick. The dipstick outer wall was dry and the tip was slightly moist. Early morning (11/4) data showed that the HTS top and bottom temperatures converged, which further indicated that most of the nitrogen liquid had evaporated. Table 1 lists the HTS temperatures and associated time, as measured by the PLC. Figure 10 is the graphic illustration of the data table.

TIME (Military)	HTS TOP (Kelvin)	HTS BOTTOM (Kelvin)
0325	119	129
0537	158	168
0813	183	184
0902	195	206
1011	214	233
1102	226	233
1200	239	242
1305	252	252
1400	262	262
1452	270	272

Table 1: HTS temperature readings as captured by the PLC system

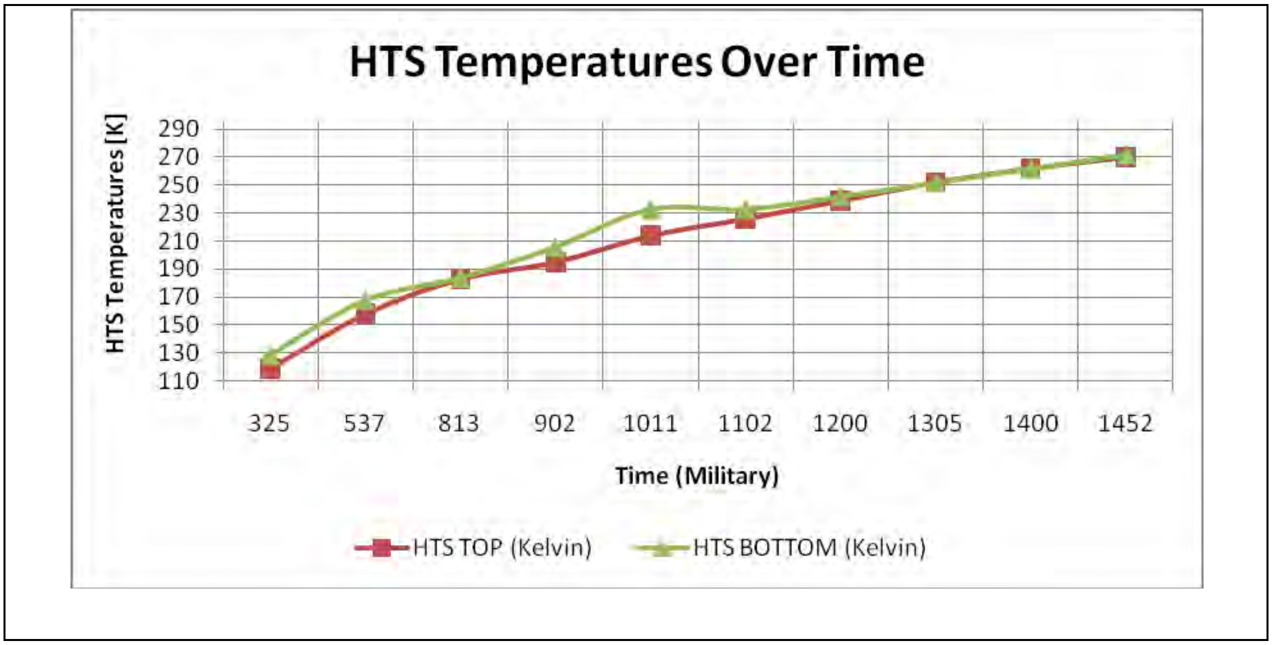


Figure 10: HTS Temperatures Rising Over Time

10 Remove Moisture and Heat to Ambient Temperature

At 10:00am a bottle of "warm" compressed nitrogen was attached to the LN2 chamber to begin warming of the space. The warm nitrogen was connected and LN2 heaters remained on, for about 5.5 hours. The heat gun was removed.

Figure 11: Compressed Nitrogen Bottle attached to get chamber at ambient temperature

At 3:40pm, we used the Endoscope to inspect the chamber for any remains of liquid. Figure 12 illustrates the position of the Endoscope probe as it was placed inside the chamber and Figure 13 shows the image on the Endoscope monitor.

Figure 12: Location of Endoscope in relation to the measurement inside chamber

Figure 13: Image on Endoscope - shows droplets of liquid on floor of LN2 chamber

11 Repairing the Electrical Plug for the LN2 Heater Wires

At this point in the process, we de-energized the LN2 heater coil. Before connected the plug back to the top lid of the chamber, we insulated the pins for the HTS coil power. Insulation was installed to prevent the chance of electrical shorting occurring across the energized pins and the loose LN2 heater pins inside the mounting hole. The copper gasket was replaced on the port and the connector was reinstalled.

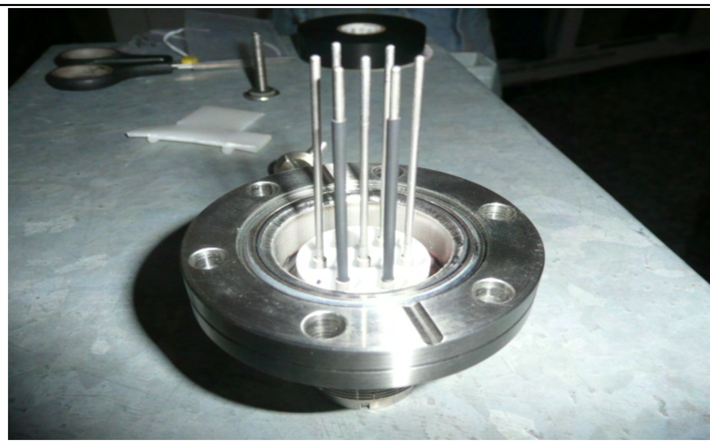


Figure 14: Insulation installed on exposed pins of connector plug

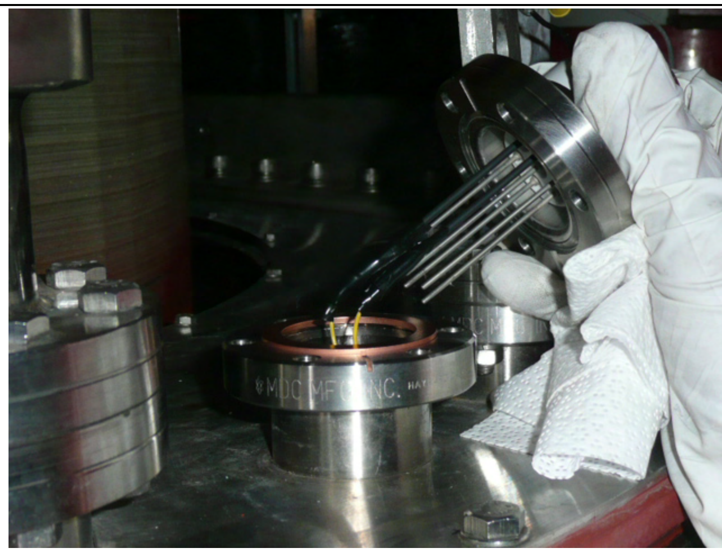


Figure 15: Plug with pins completely insulated

12 Evacuating the LN2 Chamber

At 5pm we connected two scroll pumps (provided by vendor, PTB Sales) to the LN2 chamber and began to evacuate the chamber down to 1mTorr, to reach proper vacuum for the Cold-Head test and to ensure that the moisture was completely removed. Figure 16 is an image of the pumps connected and the “warm” nitrogen compressed air still attached.

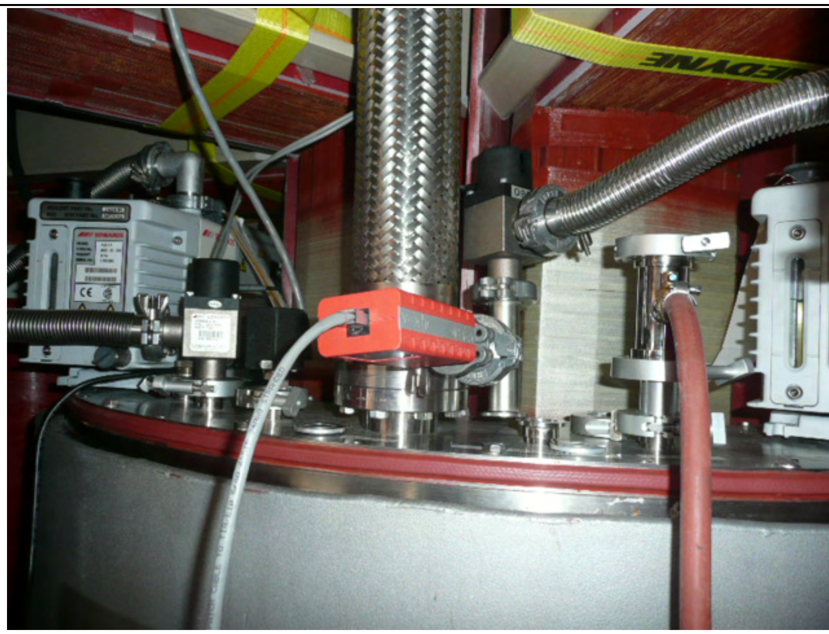


Figure 16: (2) Edwards 20cfm Scroll Vacuum Pumps were installed in the system

Pumps ran on the system overnight, and by morning the vacuum in the system was 2.9mTorr, as displayed in Figure 17. Turbo pump was then attached to the system and further vacuumed the chamber to 2mTorr.

Figure 17: Vacuum level at 9AM 11/5

13 Conclusion

The LN2 was successfully evaporated with this process, as well as all the moisture removed from the chamber. The internal vacuum level was at ~2mTorr after final pumping.

14 References

MSDS No. P-4631-H, Praxair, Inc.

15 Index of Figures

16 Index of Tables

APPENDIX I:
Zenergy Power HTS FCL Liquid Nitrogen Fill Procedure

Report

FCL-CEC: **Error! Reference source not found.**

June 2011 2010

ZENERGY POWER

www.zenergypower.com

Confidential & Proprietary

Report

Status (Final or Draft):	Final

Reporting Entity:	Zenergy Power Inc. 379 Oyster Point Boulevard, Suite 1, South San Francisco, CA 94080 USA		
Responsible Person:	Christoph Linden		
Project Name:	FCL-CEC		
Document Title:	FCL-CEC: Preparation / **Error! Reference source not found.**		
Document Ref. No.:	ZP/ES-2009-XXA < Assigned by Erica		
Date of issue:	11/04/2009		
Client(s):	Southern California Edison, Shandin Substation		
Author(s):	Christoph Linden	Approved:	Christoph Linden
Distribution:			
Summary			

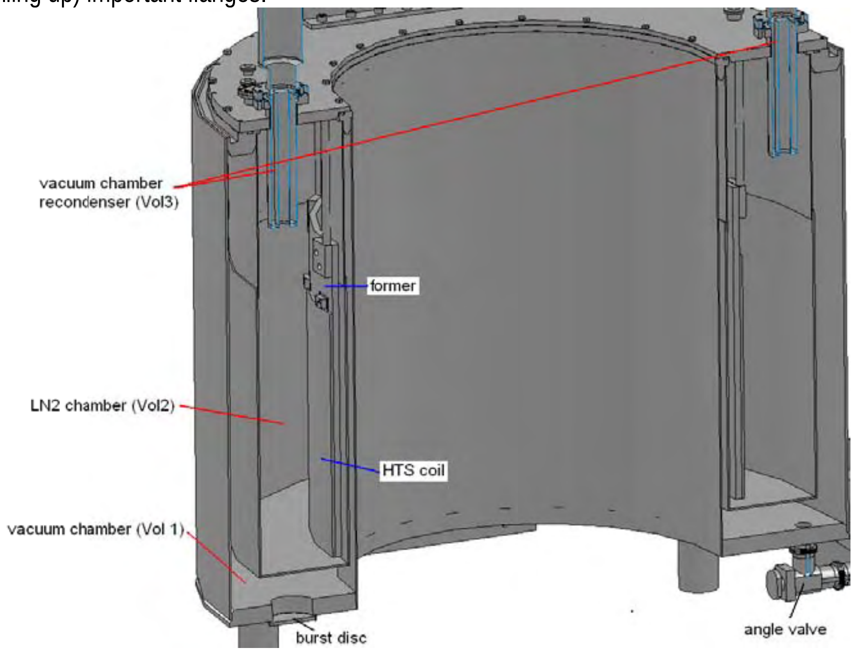
List of Revisions

Revision	Date	Action	Modified Page
A	MM/DD/YY	Initial Release	

Contents

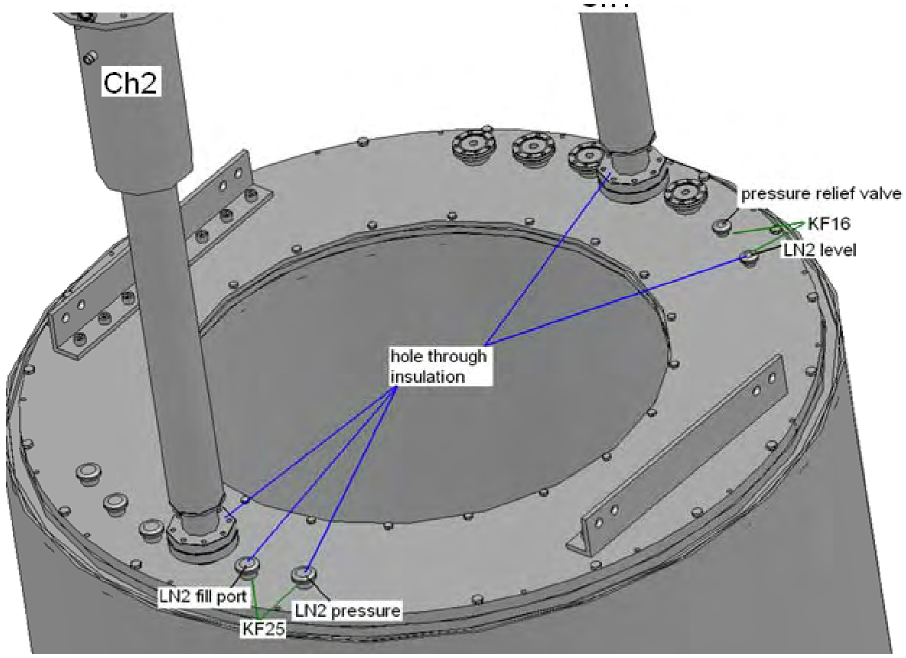
1 Introduction / basic information

Before the description of preparation and filling up liquid nitrogen into the system, here is an overview over the system, its chambers and (for filling up) important flanges.



Picture 1: overview chambers of the system

Volume 2 is the chamber, which is filled up with liquid nitrogen. Inside this chamber there is the HTS coil and its former. Volume 1 and the volumes 3 are chambers that are evacuated to avoid heat getting in the system due to convection and thermal conduction.



Picture 2: Overview of important flanges for filling up

The important flanges to fill up volume 2 with liquid nitrogen are “LN2 fill port” and “LN2 pressure”.

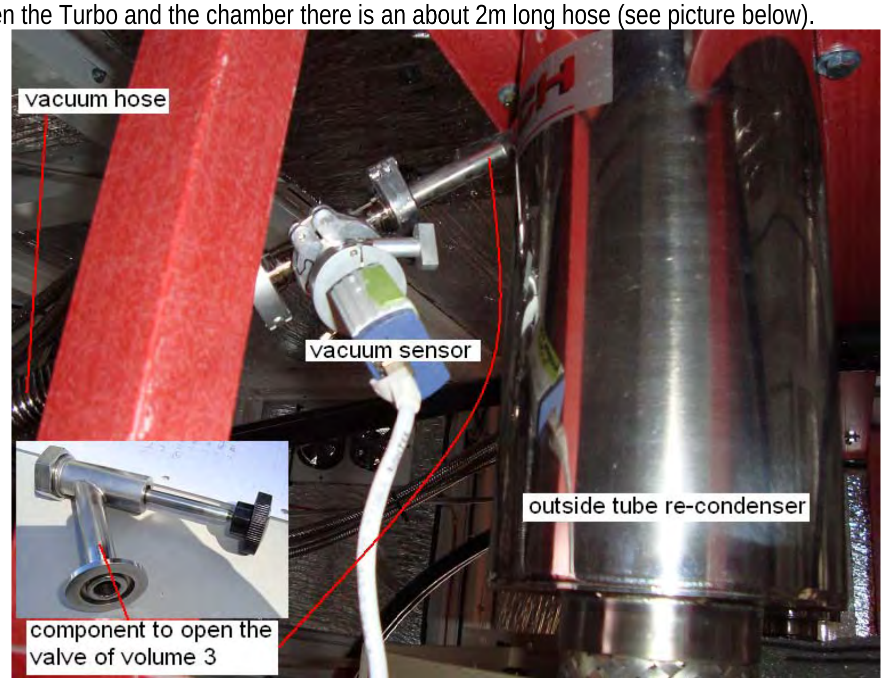
2 Preparation

During the leak detection of the system (see report of the leak detection), we evacuated volume 1 and the two volumes 3. As you can read in the introduction, the evacuation of these chambers is necessary to create an insulation vacuum for the system.

Volume 1:
The vacuum pressure we reached in volume 1 before starting to fill up volume 2 was $p = 1{,}5 \cdot 10^{-4}$ mbar. We measured this value with the vacuum gauge "Atmion", which we assembled at the angle valve of volume 1. (For more information about the new assembled parts of the system, please see the report of the leak detection). This pressure is good enough to start the fill up process. If the surfaces then get cold, the pressure will decrease further due to freezing molecules at the cold surfaces. You will see this effect later in this report (chapter "filling with liquid nitrogen").

Information:
The vacuum inside volume 1 was first in the range of 10^{-2} mbar as we opened the valve of the chamber.
The vacuum, we reached after pumping down the volume a few days was in the range 10^{-4} / 10^{-5} mbar. As we closed the new angle valve then, the pressure increased a little bit. This behavior is normal, because there is no more pumping effect to the molecules and the sensor, if you close the valve. But we saw also, that the pressure increased for example after leak testing and disconnecting the leak detector (leakage rate of vol.1: $<1{,}0 \cdot 10^{-8}$ mbar·l/s) from $3{,}1 \cdot 10^{-3}$ mbar to $3{,}5 \cdot 10^{-3}$ mbar in 5 hours. With this leakage rate of volume 1 it would normally take 26 days to increase the pressure in this way. The only possibilities of this effect are for example outgassing of some materials and a desorption of molecules due to a increasing outside temperature. To keep the pressure of $1{,}5 \cdot 10^{-4}$ mbar before filling we pumped down this chamber as long as we could and stopped short before starting the fill up process.

Volume 3:
The vacuum pressure we reached in volume 3 surrounding re-condenser 1 was $p = 7{,}3 \cdot 10^{-3}$ mbar.
The vacuum pressure we reached in volume 3 surrounding re-condenser 2 was $p = 1{,}6 \cdot 10^{-2}$ mbar.
These values were measured with a sensor that was connected directly to the volume. The problem of not getting a lower pressure depends on the long distance between Turbo pump and volume 3. There is no way to fix the Turbo directly to volume 3. Between the Turbo and the chamber there is an about 2m long hose (see picture below).



Picture 3: Evacuation of volumes 3

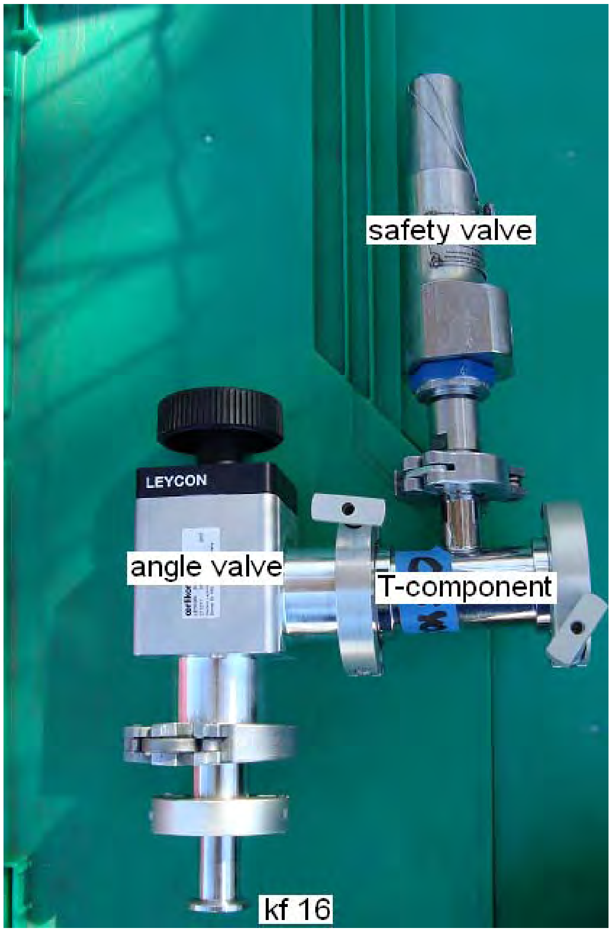
Because we don't have a vacuum gauge at these chambers and we could not check for leaks at the valves of the volumes 3, we installed a temperature sensor to the outside tube of re-condenser 1 (see picture below). With the measured temperatures we can check, if there is still an insulation vacuum during the operation of the machine.

Picture 4: Temperature sensor at the outside tube of the re-condenser

Information:
The vacuum inside both volumes 3 was first in the range of 10^{-1} mbar as we opened the valves of the chambers. To reach the pressures (described on page before), we pumped down half a day with the pump station of the US colleagues (forepump and Turbo). Like the company of leak detection said, they did not pump down the volumes 3 with a separate pump station, instead they only used the integrated pumps of the leak detector. With these integrated pumps, we saw at the current leak detection, you reach a pressure in the range of 10^{-1} mbar of the volumes 3. So during the last operation of the machine there was a starting pressure from only 10^{-1} mbar, which could have been a problem.

Safety valve:

Because we found a leak at the safety valve (old and new one), we wanted to have an assembly, which makes it very easy to change the valve during the operation without opening volume 2. On the following picture you see this assembly, we built before starting to fill up volume 2.



Picture 5: new assembly of safety valve

During the operation the angle valve must be open to have the safety valve working. If you want to change the safety valve because of the leak we found, you can do this during operation with closed volume 2. For it you have to close the angle valve, switch the current valve with a new one and open again the angle valve.

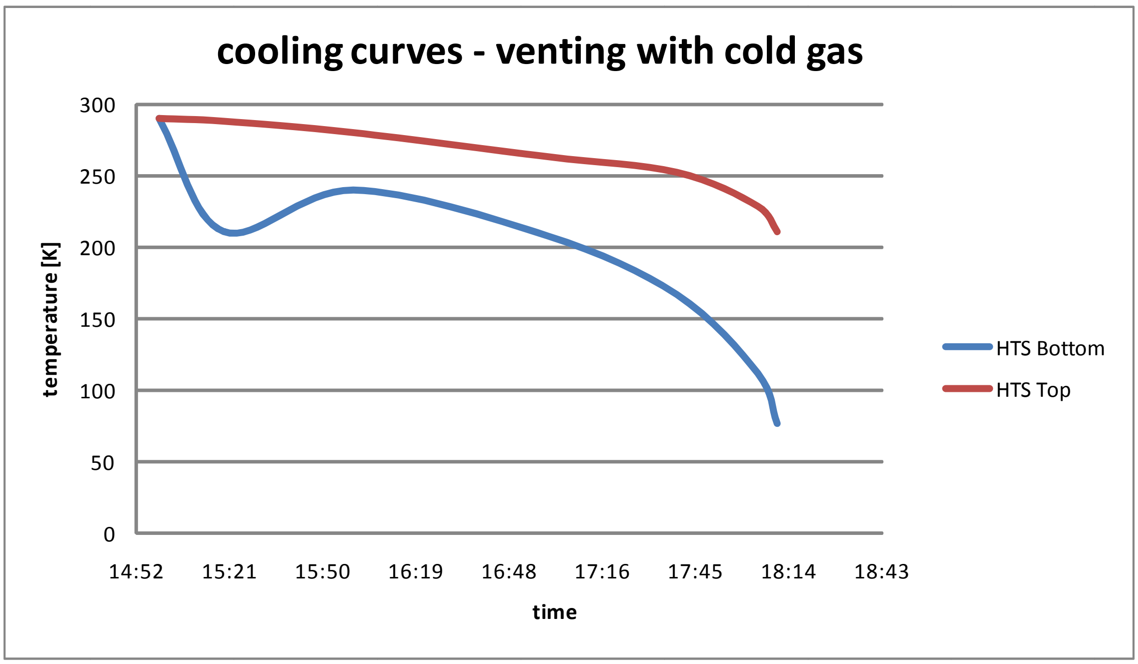
After this last preparation and after finishing the leak detection we started the process of filling up volume 2 with liquid nitrogen. This process is described in the following chapter.

3 Filling with liquid nitrogen

1.) We started our fill up process with opening the flanges “LN2 fill port” and “LN2 pressure”. The flange of the safety valve was still open (only plastic cap), we left it open and removed the plastic cap.

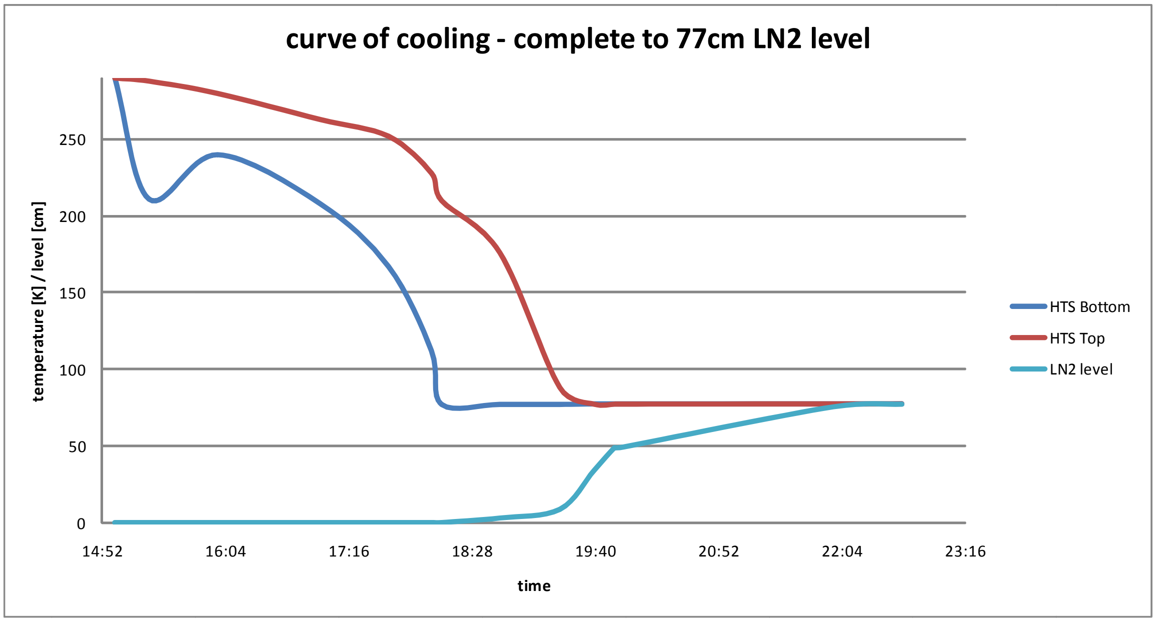
2.) After preparing the chamber we connected a red rubber hose to the first dewar (liquid outlet) and inserted the hose to the “LN2 fill port”. (information about choosing the rubber hose you can read in manual of filling up with liquid nitrogen)

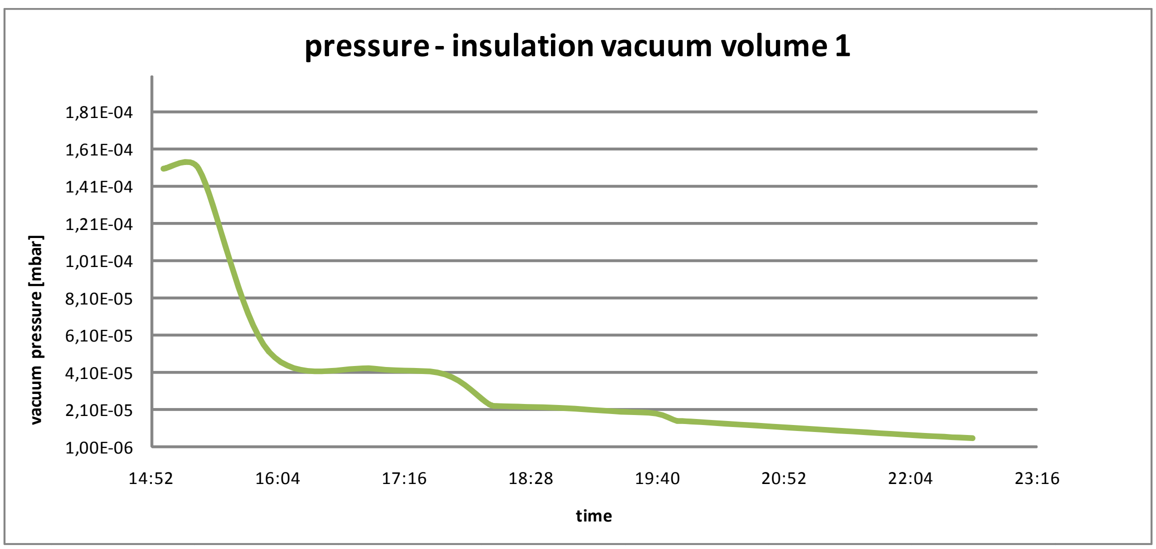
3.) We opened the liquid outlet a little bit and cooled down volume 2 with a slow flow of cold nitrogen gas. During this venting with nitrogen gas we left the safety valve flange open to have circulating flow through the chamber (To open this flange is not so important, we left it open, because it was already). In the following diagram you can see the cooling process with the cold gas and a very low rate of temperature reduction.



In this diagram you see that we inserted the hose to the bottom of the chamber. The first minutes we opened the dewar too fast, so that the HTS bottom temperature decreased too fast down to 220K. That’s the reason we adjusted the dewar outlet again so that you can see constant and slow temperature reduction at about 4pm. The average temperature decreasing during this venting with cold nitrogen gas is 48K/h. We took a time of 3 hours to cool down the HTS Bottom with cool gas only to 77K.
At 5pm we mounted the safety valve-assembly to close the KF16-flange. We closed this flange, because we wanted no more cycling gas from this point but a faster subcooling. The other flanges “LN2 fill port” and “LN2 pressure” are still open.

4.) At this point we opened the liquid outlet of the dewar more and more to reach a faster subcooling. Additionally we connected a second hose to a second dewar liquid outlet to accelerate the filling process now. At this temperature level and the opened outlets of two dewars we get more and more liquid nitrogen into the chamber. In the following diagrams you see the complete cooling curves, the liquid nitrogen level in volume 2 and the pressure of volume 1.





You see that it took us about 8 hours for the complete subcooling and filling process. We filled up the LN2 to a level of 77cm. During this time the insulation vacuum of volume 1 decreased to a range of 10^{-6} mbar. We filled up the liquid nitrogen in several steps (50cm, 60cm, 70cm, 72cm…77cm). Every step we closed both dewars and checked the level with a endoscope through “LN2 fill port” (see the manual of filling liquid nitrogen for further information about checking the level with an endoscope and the maximum level). With a level of 77cm we were about 1cm under maximum level.

5.) After reaching and checking the level, we pulled out the hoses and got rid of the ice at the flanges with the heat gun. We cleaned all sealings and components to close the flanges later.

6.) Now we turned on cold head 1 and missed unfortunately the 80K point to close the flanges of the chamber. We saw that there was no more venting of the nitrogen gas out of the open flanges, instead there was already a little underpressure in volume 2. The coldhead reached 67K at this moment.

7.) Because of missing the closing point, we turned off cold head 1 and saw the nitrogen gas venting out of the open flanges again, when the cold head reached about 79K. For getting out the air that was sucked in because of the underpressure we let vent the nitrogen gas for about 20 minutes. We think that in this short “underpressure time” not all of the air freezes directly out at the cold surfaces, so that we can vent it out.
Due to the venting, we refilled the lost liquid nitrogen with one hose to 77cm. During this time the temperature of the turned off cold head on increased to about 100K.

8.) We cleaned up again all components and sealings, melted the ice on the flanges and restarted cold head one. This time we closed both flanges (“LN2 fill port” and “LN2 pressure”) over a temperature of 80K of cold head one.

The following steps and tests we did to cool down the liquid nitrogen bath you can read summarized in the presentation “Zenergy Power – FCL CEC - exactly history of testing by remote in SF” and the word documents “cool down of cryostat (2)”.

APPENDIX J:
Silicon Power SSCL Test Plan

Test Plan

For

15kV 1200A

Solid State Fault Current Limiter (SSCL)

For Field Evaluation Testing

At

Southern California Edison (SCE)

Revision 2 – August 15, 2008

Prepared by

Mahesh Gandhi, Ph 484-913-1520

Silicon Power Corporation, Malvern, PA

CONTENTS

LIST OF FIGURES

1 INTRODUCTION

The increase in available fault current levels due to added distributed generation and increased load has stressed many transmission and distribution substations to their limits. In some cases fault current levels are exceeding the interrupting capability of existing substation circuit breakers. This increase in fault current levels either requires the replacement of large numbers of substation breakers or the development of some means to limit fault current. By using a Solid State Current Limiter (SSCL), fault currents can be limited well before it reaches the ***1st peak*** and to the desired value ***within ¼ cycles (4ms)***. This will allow near instantaneous breaking of bus ties in transmission and distribution substations to reduce the available short circuit current and allow existing circuit breakers to clear at lower fault current levels.

When new capacity, such as the additional generation created by independent power producers, is merged with existing power systems, higher levels of fault current is introduced in the system. The increased fault current can cause failure of circuit breakers at a substation if they exceed their fault clearing or breaking ratings. While the breakers might be replaced with higher-rated equipment, this solution may not be economical or viable due to space constraints, and the difficulties associated with outages necessary for replacement may be severe. This device will provide performance similar to a circuit breaker, but with the added function of current limiting. Unlike a circuit breaker, the SSCL will act to limit high current faults even before the first current peak is reached. This limiting effect is provided well before interruption of the fault occurs. Whereas a high speed circuit breaker typically interrupts high current faults in about two and a half cycles, the SSCL will interrupt them after one-half cycle. SSCL can be an even better environmental alternative to the use of breakers, which employ greenhouse gasses (SF6).

SSCL offer many other benefits such as:

New Capacity - Solid-state current limiters could be applied to new capacity additions and/or “surgically” at strategic locations, such as substation bus ties, to effectively mitigate the fault current from multiple generation sources. This would provide a flexible tool that could be used to accommodate new capacity from generation or transmission distributed or aggregate generation energy storage.

Grids Operations Alternatives -The new functionality made possible by the flexibility of power electronics will also enable innovative alternatives in operation of the grid. For example, power electronics can mitigate unexpected load increases or major asset failures with temporary generation, protect “line commutated” FACTS devices from close proximity solid state s and improve the performance of superconducting cables.

Superconducting Cables - A solid state current limiter added in series with a superconducting cable can improve the cable's performance and enable design of smaller cable sizes, as well as eliminate loss of superconducting cable operation during cryogenic recovery time following an external fault. The insulation system of a superconducting cable is likely to have limited strength because of the need for minimal mechanical cross section bracing spanning the vacuum segment. It may not be capable of handling the magnetic forces occurring in the worst case of a high current fault, particularly in transmission applications, which will draw fault currents from higher impedance parallel paths. The solid state current limiter will be an essentially enabling adjunct to the regular use of superconducting cables.

Inrush Current - The Solid State Current Limiter has a unique capability to limit inrush current, even for capacitive loads, by gradually phasing in the switching device. This may be of particular benefit in mitigating stress on generator shafts, while preserving the reliability benefits of multi-shot reclosure on generator buses, particularly as distributed generators are deployed at various voltage levels and locations across utility grids.

Open Access - Because of the critical role of solid state current limiting as an early enabler within EPRI/DoE's Roadmap Document to support "open access," transmission and generation capacity increases, energy storage needed for improved asset utilization and renewable economics, distributed and aggregate generation, this new functionality is also being pursued in a parallel development effort for transmission level solid state current limiters using superconducting and other technologies.

In 2000 EPRI began a project to develop a solid state current limiter (SSCL). A three phase, 15 kV, 1200 A, distribution class prototype SSCL has been constructed and underwent design tests. The design uses the Thyristor as main switching devices. The next steps will be to (1) design SSCL to incorporate the latest device technology and experience gained to date and then (2) subject this updated and improved unit to a field trial.

At present no real world field application experience exists for the EPRI developed solid state current limiter (SSCL). This information is vitally needed by the utility community to effectively apply and operate the SSCL. Areas that need to be studied include electrical and mechanical performance, reliability and availability, maintainability, effectiveness of power quality enhancement, and coordination with existing power system components. This will give the design team information about any needed improvements and will provide evidence to utilities that the SSCL is a practical reality.

The objective of this phase of program is to conduct a field trial of a medium voltage SSCL. SPCO will deliver One (1) 15kV 1200A. The SPCO SSCL design uses advanced power semiconductor technologies, latest electrical components and insulating materials and state of the art manufacturing practices. The unit will be field evaluated at Southern California Edison.

This document provides detail test plan of test to be performed on unit at factory and at field. The sections includes list of tests, detail test procedures, and test schedule.

2 SSCL DESIGN

2.1 SSCL Design

The SSCL design is modular and scalable. It is based on a standard building block which can be stacked to get the desired voltage and current ratings. On the 15kV SSCL the power stacks will be submerged in a cooling and insulating liquid. The overall design will be similar to a liquid cooled outdoor transformer. It will have cover-mounted power bushings for ease of connections. The tank shall have sufficient mechanical strength for the years of service and to withstand environmental conditions. The tank shall have accessories like: liquid level gauge, liquid temperature gauge, pressure vacuum gauge and pressure-relief device, control cabinet mounting, and cooling radiators.

2.2 Standard Building Block

In order to facilitate manufacturing, and reduce the maintainability and the ownership cost of the unit, standard-building blocks – Voltage Level Blocks – concept is approached. Each of these building blocks is a complete SSCL switch rated to up to 2kA and about 5kV blocking, and resembles a fully functional SSCL. The needed number of series levels is determined by the breakdown voltage of the main switch modules and the arrestor voltage. SGTO die are typically rated at 6.5kV, although, at present modules containing these die are very conservatively rated to 5kV. Because resonant turn-off is so benign, there is virtually no voltage overshoot of the arrestor allowing it to be set as high as 4.5kV.   We have selected 4kV for the 15kV SSCL.

The physical arrangement for the building block is depicted in Figure 2-1.

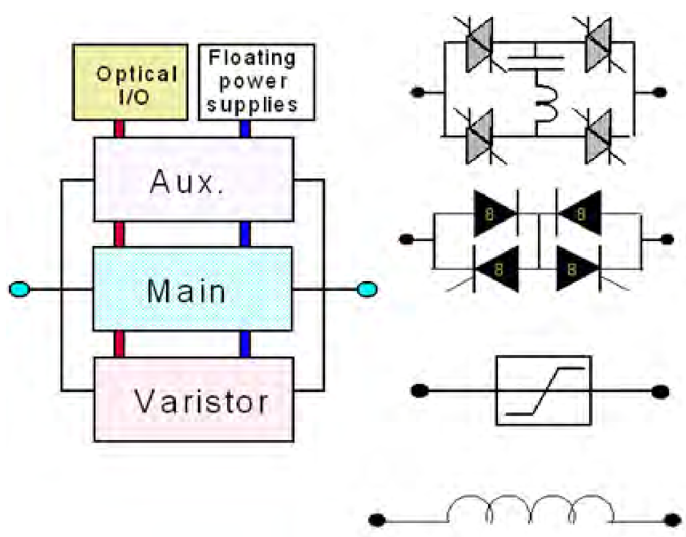


Figure 2-1 Voltage Level Building Block

The Figure 2-2 provides the detail mechanical layout of the key level block elements. The Main and the Aux SGTO switch modules will be mounted on a common heat sink, which provides the mechanical backbone of the level block. The resonant capacitor is placed at one end of the heat sink and four varistors and the Current Limiting Inductor (CLI) at the other. This forms a 5kV 1500A Building Block.

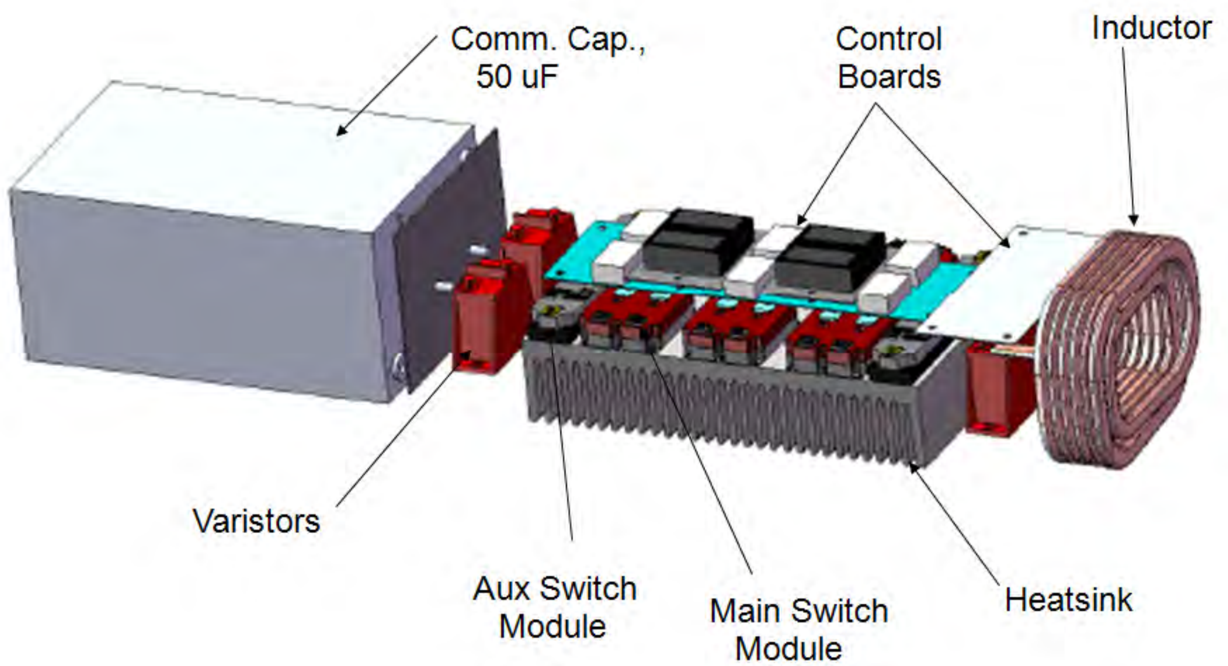


Figure 2-2 Voltage Level Building Block, 5kV 1500A

2.3 Standard Power Stack

The number of levels in series, N, is then based on assuring that the average varistor losses during worst case limiting operation are well within their ratings. The number of series Voltage Level Blocks (VLB's) is first governed by the transient blocking voltage rating and the margin chosen between that voltage and the arrestor voltage (at 9 kA current). 15kV SSCL will have 10 of the 5kV (blocking voltage) 1500A units per phase, all stacked in series. The stack assembly is seen in Figure 2-3.

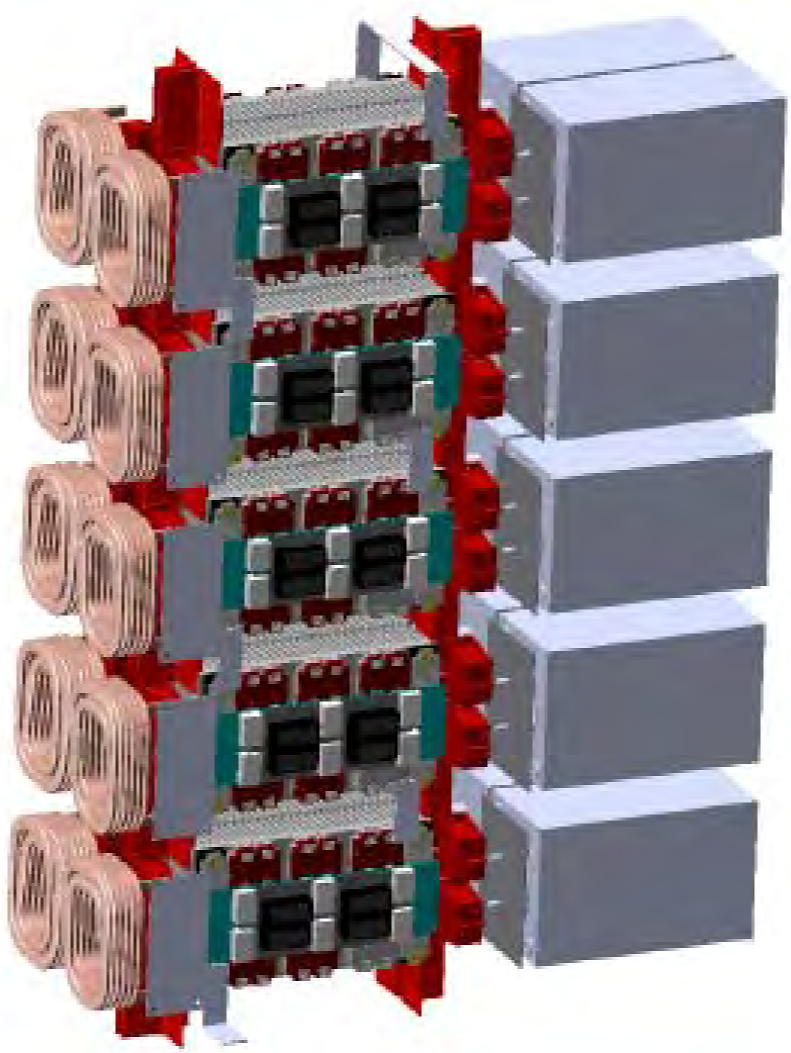


Figure 2-3 Stack Assembly, 15kV 1500A

2.4 Final Packaging

The system is packaged as one 3-phase assembly. It can be seen in Figure 2-4 that one stack makes a single phase and 3 such are placed in a single tank filled with oil for cooling.

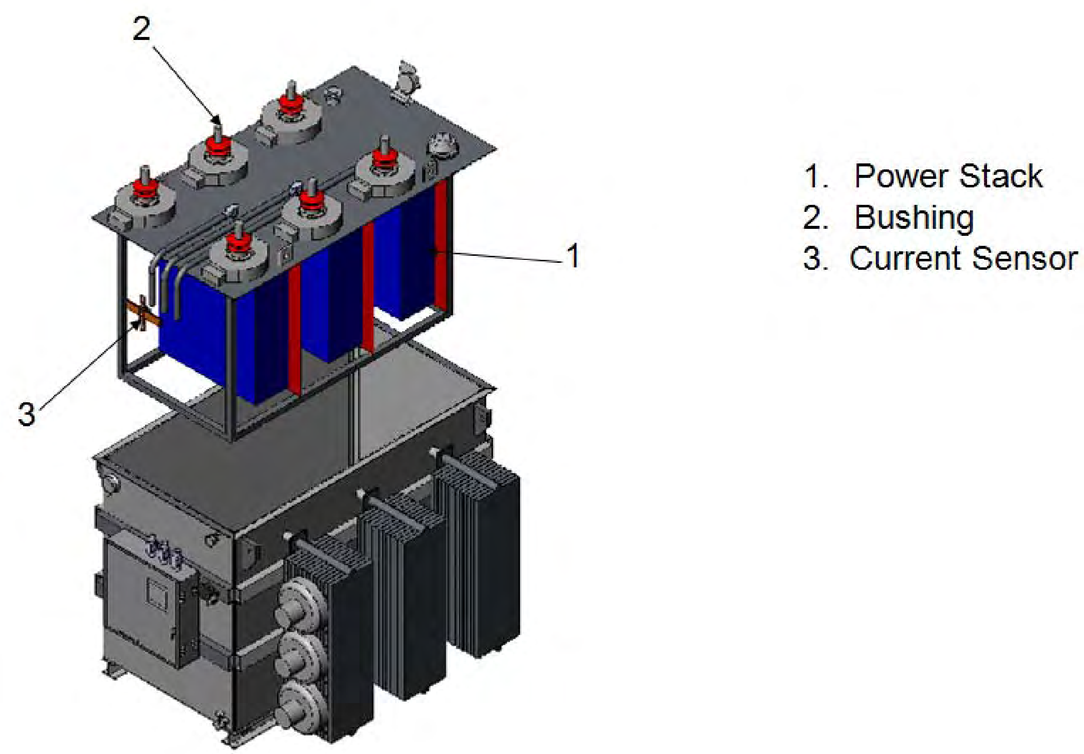


Figure 2-4 Tank Assembly

2.5 SSCL Accessories

The SSCL will be provided with the accessories shown in figure 2-5.

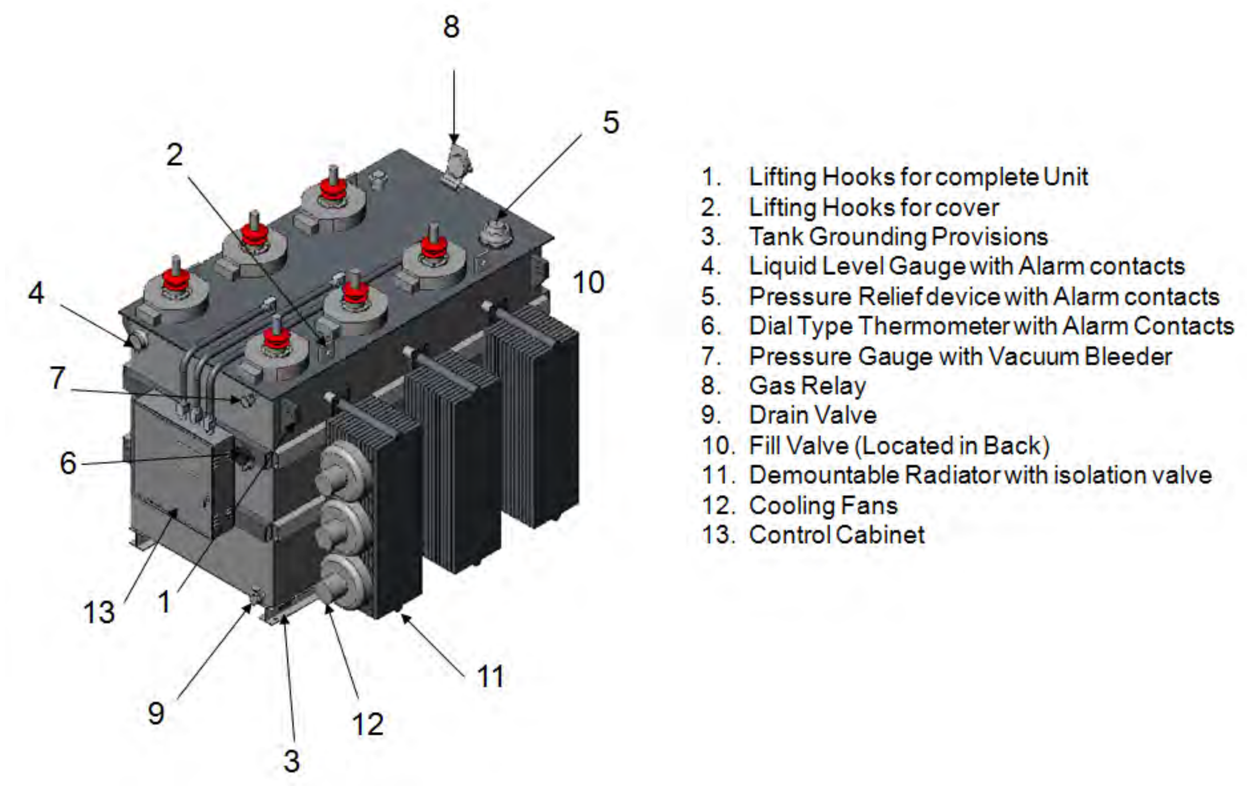


Figure 2-5 SSCL Accessories

2.6 Control System

The 15kV SSCL is designed to operate primarily from the remote. It also has the capability to operate locally. The controls shall include ON/OFF controls, equipment Protection, Supervisory Controls and Data Acquisition (SCADA), Display and Monitoring of Operating parameters, Fault Log, Access Protection, e-Tagout, Safety Padlocking, etc. Control and communication system shall be compatible with communication standard IEC-61850. The SSCL controls will provide a trip free feature where any close signal shall not inhibit the SSCL from opening upon command.

The communication between the VLC boards and the trip controller is provided with the help of fiber optics as shown in figure 2-6.

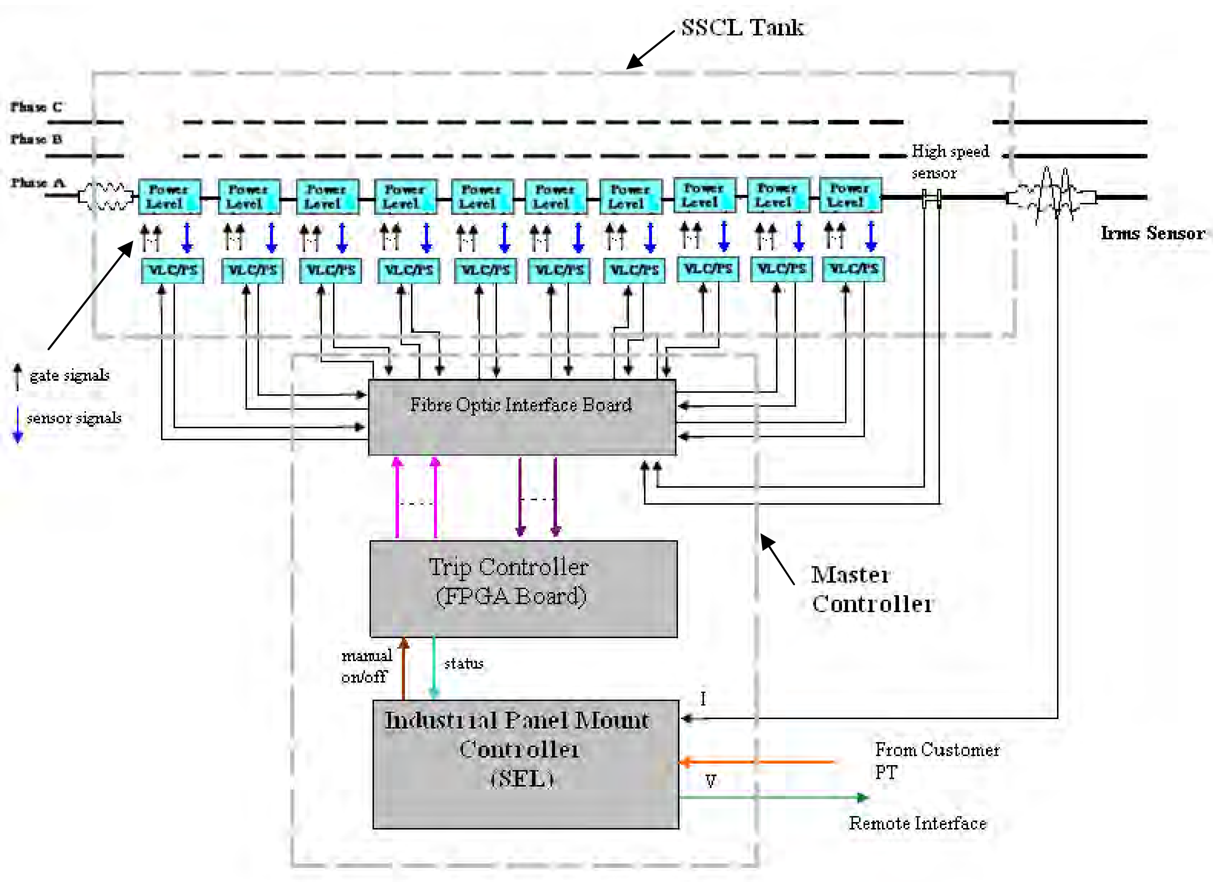


Figure 2-6 Control Architecture

The main components involved in the control system are: High Speed dI/dt Sensor, Bushing mount CT, Industrial Panel Mount Controller, Trip Controller, VLC/ PS Board and Gate Drive Boards.

2.7 Auxiliary Power Architecture

Another aspect of the SSCL is its modular power supply to the control and gate drive boards. Each power module is designed as a floating power supply. This allows necessary isolation of the modular power system from the earth ground. The externally powered module requires isolated AC voltages from the substation external power that meet the required isolation level.

The power supply input is from the station aux supply of 120V ac. The concept of the power supply design is to use an inverter that supplies high frequency transformers with necessary isolation. These high frequency transformers further feed the toroidal power supply transformers at the building block level. Figure 2-7 shows the auxiliary power supply architecture.

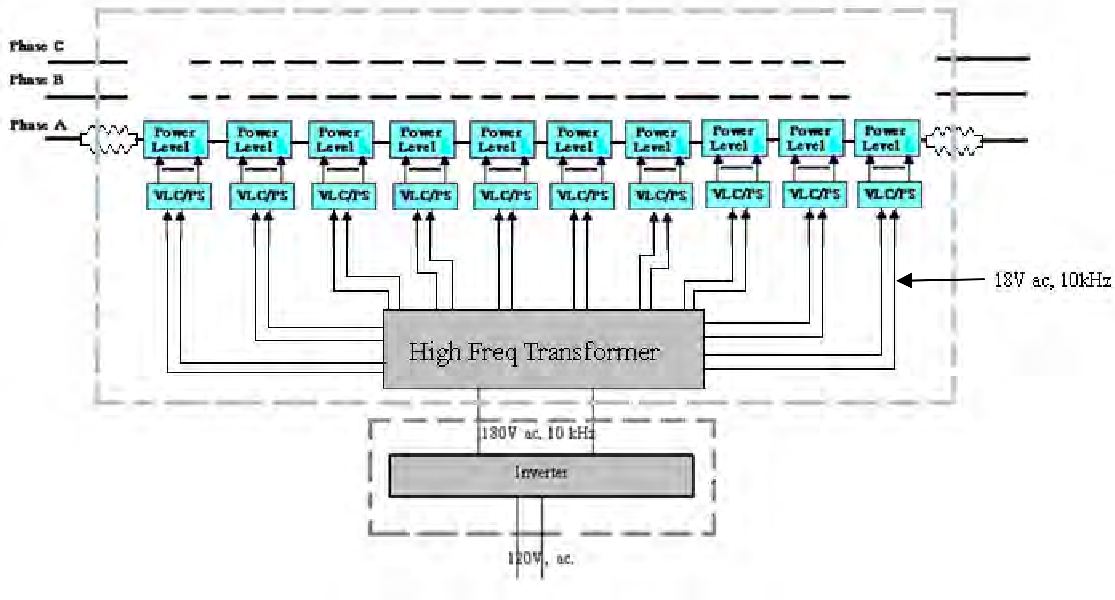


Figure 2-7 Auxiliary Power Supply Architecture

3 SSCL SPECIFICATIONS

Parameters	*Rating/Specification*
• **Rated Maximum Voltage, kV rms**	**15.5**
• **Rated Maximum Continuous Current, Ampere rms**	**1200**
• **Rated Power Frequency**	**60**
• **Available fault current, kA rms**	**23**
• **Rated Let-thru Current, kA rms**	**9**
• **Rated Let-thru Current Duration, cycles**	**30**
• **Rated Dielectric Withstand**	
– **Power Frequency 1 min dry kV, rms**	**50**
– **Impulse, Full-wave Withstand, kV peak**	**110**
– **Impulse, Chopped Wave (2uS) Withstand, kV peak**	**142**
– **Partial Discharge at 16.5kV, pC**	**100**
– **Rated Power Factor Measurement**	**?**
– **Rated Insulation Resistance at 500V DC Megohmeter**	**13000 M-ohm**
• **Ambient Temp, Degree C**	**-30 to +50**
• **Rated Control Power, V AC**	**120**
• **Efficiency Goal**	**99.75%**
• **Audible Noise at 6 feet, dB**	**68**
• **Radio Influence Voltage**	**?**

Note: Ratings based on ANSI C37-04, C57.16, C57.12.01, C57.12.90 and Customer Comments

4 LIST OF TESTS

4.1 Component Level Tests

The tests in this section will be performed at the component level.

4.1.1 Current Limiting Reactor

4.1.1.1 Let Through Current/MMF Test

4.1.1.2 DC Resistance Measurement Test

4.1.1.3 Winding Resistance Measurement

4.1.1.4 Winding Impedance Measurement

4.1.1.5 Turn-to-Turn Test

4.1.2 Auxiliary Power Supply Transformer

4.1.2.1 Isolation test

4.1.2.2 Loading test at rated kVA

4.1.2.3 Continuous operation/Temperature rise test

4.1.3 Auxiliary Power Supply Inverter

4.1.3.1 Continuous operation test

4.1.3.2 Insulation/Isolation test

4.1.4 Standard Building Block (Power Block)

4.1.4.1 Current interruption Test

4.1.4.2 Continuous Current/Temperature Rise Test

4.2 Design Verification Tests (Controlled Testing)

These tests will be performed on the SSCL unit.

4.2.1 Dielectric Test

4.2.1.1 Power frequency Voltage Withstand Test

4.2.1.2 Full-wave lightning impulse withstand voltage tests

4.2.1.3 Chopped wave lightning impulse withstand voltage tests

4.2.1.4 Partial Discharge

4.2.1.5 Insulation Power Factor Measurement

4.2.1.6 Insulation Resistance Measurement

4.2.2 Current Limiting Test

4.2.3 Efficiency Test

4.2.4 Continuous Current Carrying Test/ Temperature Test

4.2.5 Audible Noise Test

4.2.6 Radio Influence Voltage (RIV) Test

4.2.7 Electrical noise/EMI Test

4.3 Testing at SCE

These tests will be performed on the SSCL unit by SCE with the support of Silicon Power.

4.3.1 SSCL Interfaces

4.3.2 Acceptance Test at SCE

4.3.2.1 Winding Resistance Test

4.3.2.2 Winding Impedance Measurement

4.3.2.3 Turn to Turn Test

4.3.2.4 Total Loss Measurement Test

4.3.2.5 Voltage-freq Withstand Test

4.3.2.6 RIV Test

4.3.2.7 BIL Test

4.3.2.8 Chopped-wave Test

4.3.2.9 Audible Noise Test

4.3.2.10 Partial Discharge Test

4.3.2.11 Insulation Resistance Measurement

4.3.2.12 Fault current Limiting Test followed by Normal Operation Test

4.3.3 Field Evaluation Testing at Shandin Sub-station

4.3.3.1 Pre-connection Testing

4.3.3.1.1 External Inspection

4.3.3.1.2 Tank Pressure

4.3.3.1.3 Winding Resistance Measurement

4.3.3.1.4 Winding Impedance Measurement

4.3.3.1.5 Insulation Power Factor Test

4.3.3.1.6 Insulation Resistance

4.3.3.2 Field evaluation tests

4.3.3.2.1 Operational Test (Steady-state & Transient)

5 TEST PROCEDURES

5.1 Component Level Tests

5.1.1 Current Limiting Inductor Test

5.1.1.1 Let Through Current/MMF Test

The let through current of 9000A for 0.5 sec will be passed through the inductor and the MMF handling capability of the inductor will be tested.

5.1.1.2 DC Resistance Measurement Test

The DC resistance will be measured between the terminals of the inductor.

5.1.1.3 Winding Resistance Measurement

The resistance will be measured between the terminals of the inductor.

5.1.1.4 Winding Impedance Measurement

The impedance will be measured between the terminals of the inductor.

5.1.1.5 Turn to Turn Test

The insulation between the turns will be measured for the inductor.

5.1.2 Auxiliary Power Supply Transformer

5.1.2.1 Isolation Test

The Transformer will be tested for its isolation at the KEMA power labs. Isolations up to 3kV will be tested.

5.1.2.2 Loading Test

The transformer will be loaded to its rated VA that is 51VA

5.1.2.3 Continuous Operation/Temperature Rise Test

The transformer will be tested for continuous operation and the temperature will also be monitored.

5.1.3 Auxiliary Power Supply Inverter

5.1.3.1 Continuous Operation Test

The Inverter will be tested for continuous operation

5.1.3.2 Insulation/Isolation Test

The Insulation test up to 3kV will be performed at the KEMA power lab.

5.1.4 Standard Building Block (Power Block)

5.1.4.1 Current interruption test

The building block will be tested at 5000A peak from a 23kA rms available fault current at the KEMA power labs.

5.1.4.2 Continuous Current/Temperature Rise Test

The Building Block will be tested at a continuous current of 1200A rms at a low voltage at the KEMA power labs.

5.2 Design Verification Testing (Controlled Tests)

5.2.1 Dielectric Test

Objective: The dielectric integrity of a SSCL is demonstrated by subjecting it to a power frequency, a lightning impulse test, and where required, a chopped wave lightning impulse and a switching impulse test.

5.2.1.1 Tests conditions

a) Dielectric Voltage Withstand tests on SSCL shall be made under atmospheric pressure, temperature, and humidity conditions normally prevailing at the testing facility.
b) The SSCL shall be clean and in good condition, and shall not have been put into commercial operation.
c) Correction factors shall not be used on normal power frequency dry tests, unless allowed by industry standard. The values of correction factors for atmospheric pressure and atmospheric humidity to be used for impulse and power frequency wet tests are to be taken from IEEE Std 4-1978 curves and formulas applicable to atmospheric bushings, except where otherwise noted.
d) The bushing and rod gap correction factors will not always have the optimum accuracy for a specific design of SSCL. In cases where more accurate correction factors can be made available for a specific design or class of designs, they may be used.
e) When revisions in correction factors in IEEE Std 4-1978 are made, they shall be applicable to new designs only and it shall not be necessary to repeat design tests on designs for which such tests have been completed.
f) Dielectric test voltages shall be measured in accordance with IEEE Std 4-1978 voltage measurement standards.
g) For lightning impulse and chopped wave tests, atmospheric temperature and pressure correction factors shall be applied to define the test voltage. For SSCLs, the use of humidity correction factors is required (see IEEE Std C37.20.2-1993).

5.2.1.2 Insulation paths

When performing dielectric tests, two classes of insulation paths are to be considered:

1. *Atmospheric paths*: Paths entirely through atmospheric air, such as along the porcelain surface of an outdoor bushing.
2. *Non atmospheric paths*: All other paths, such as through a liquid such as oil, through a solid, or through a combination thereof.

Non atmospheric paths

In order to meet the requirements for non atmospheric paths, at least three dry withstand tests must be accumulated at each polarity, at the rated lightning impulse and related chopped wave voltages (in addition to one dry power frequency withstand test), all without benefit of reduction of voltages due to correction factors. The purpose is to apply full stresses to these non atmospheric paths; therefore, tests in which a flashover occurs through an atmospheric path may be ignored. It is permissible to raise the dielectric strength of the atmospheric paths by artificial means, such as an extra high-voltage shield or a corona ring.

In some atmospheric conditions, it may be desirable to delay testing of the non atmospheric paths until conditions improve.

Atmospheric paths

There is no separate atmospheric path requirement for the dry-power frequency test.

5.2.1.3 Power frequency withstand voltage tests

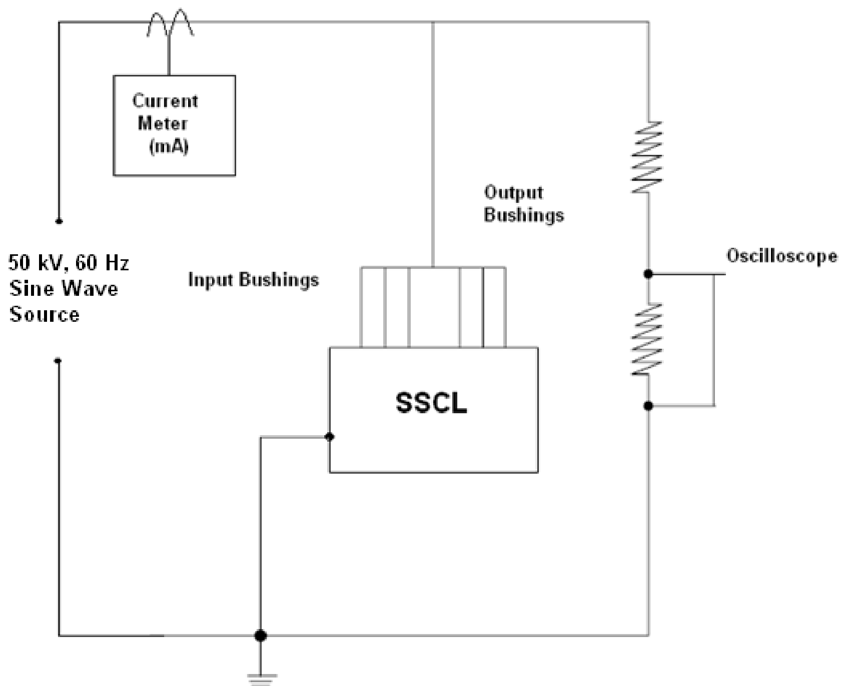


Figure 5-1 Test Schematic for Power Frequency Withstand Voltage Test

Wet test procedure

The wet tests are made only on outdoor SSCL or on external components such as bushings, in accordance with the procedure described in IEEE Std C57.19.00-1991. For those bushings, where their voltage distribution is negligibly influenced by their surroundings, and which have been tested separately as individual bushings in accordance with IEEE Std C57.19.00-1991, the tests need not be repeated in the assembled SSCL.

5.2.1.4 Full-wave lightning impulse withstand voltage tests

These tests are made on SSCL, under dry conditions, to verify their ability to withstand their rated full-wave lightning impulse withstand voltages. In these tests, both positive and negative, lightning impulse voltages having a peak value equal or greater than the rated full-wave lightning impulse withstand voltage, 110kV, shall be applied to the terminals of the SSCL.

NOTE—some insulating materials retain a charge after an impulse test. For these cases, care should be taken when reversing the polarity of the test voltage. To allow the insulating materials to discharge, the use of appropriate methods, such as the application of impulses of the reverse polarity at lower voltages (50–75% of rated value), are recommended.

Waveform for lightning impulse tests

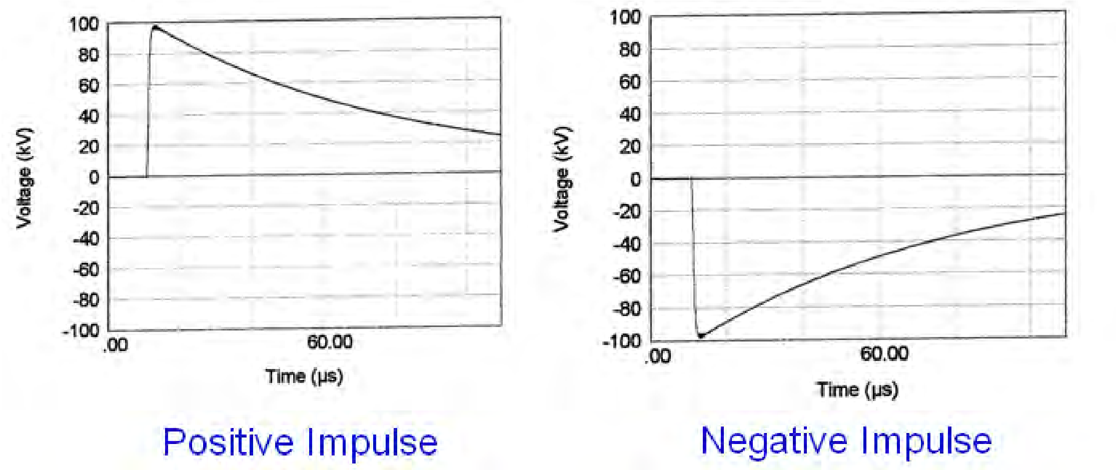


Figure 5-2 Waveform for lightning impulse tests per IEEE Std 4

The waveform and application of the full-wave test voltage shall be as described in IEEE Std 4-1978 and shall have the following limits:

a) A full-wave test voltage with a virtual front time based on the rated full wave impulse test voltage, equal to or less than 1.2 µs;
b) A peak voltage equal to or exceeding the rated full wave impulse voltage; and
c) A time to the 50% value of the peak voltage, equal to or greater than 50 µs.

If the capacitance of a test sample is too high for the test equipment to be able to produce a virtual front time as short as the 1.2 µs while maintaining the peak value, the most rapid rise possible may be used, subject to agreement between the user and the manufacturer.

Test procedure

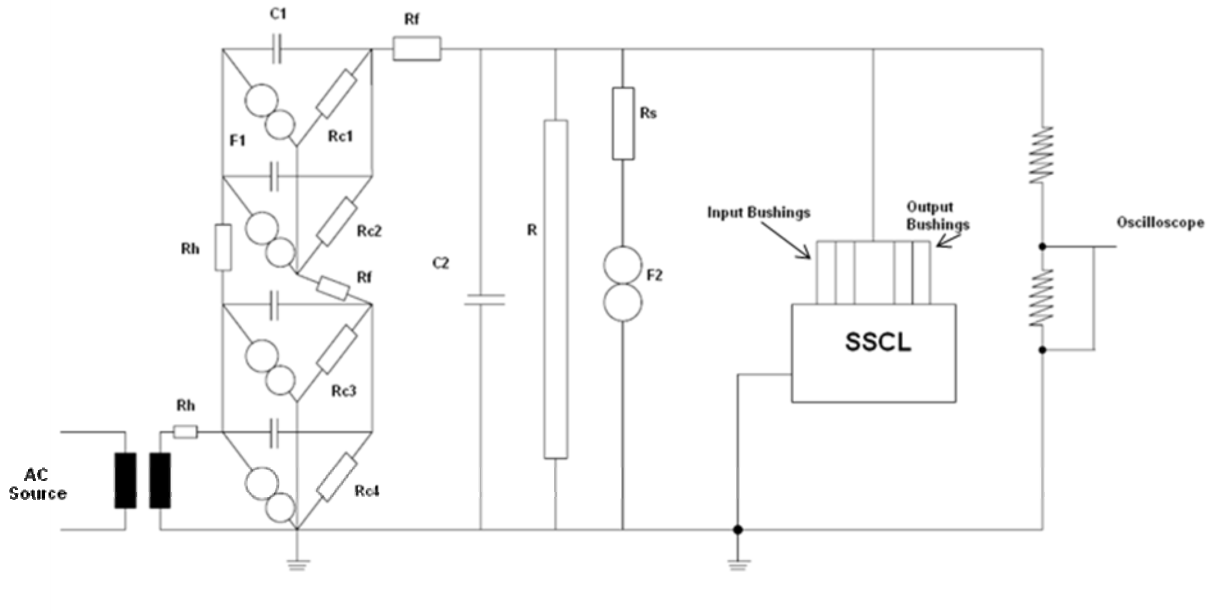


Figure 5-3 Schematic for Full Wave Impulse Test

The test procedure shall consist of the following tests performed in any order

- Apply three consecutive positive lightning impulse voltage waves individually to each phase of the circuit breaker with the other phases and the frame grounded.
- Apply three consecutive negative lightning impulse voltage waves individually to each phase of the circuit breaker with the other phases and the frame grounded.

If a flashover occurs on one of the above mentioned tests, a second group of nine tests shall be made. If the SSCL successfully withstands all nine of the second group of tests, the flashovers in the first set of tests shall be considered a random flashover and the SSCL shall be considered as having successfully passed the test.

5.2.1.5 Chopped wave lightning impulse withstand voltage tests

These tests shall be performed on SSCL that have a rated maximum voltage of 15.5 kV and above to verify their ability to withstand their assigned rated chopped wave lightning impulse withstand voltage.

The magnitude of this voltage is 142kV. It shall be applied to the terminals of the SSCL, without causing damage or producing a flashover, following the same procedure as described in 5.1.1.4.

The waveform and application of the chopped wave test voltage, and the type of rod gap and its location, shall be as described in IEEE Std 4-1978.

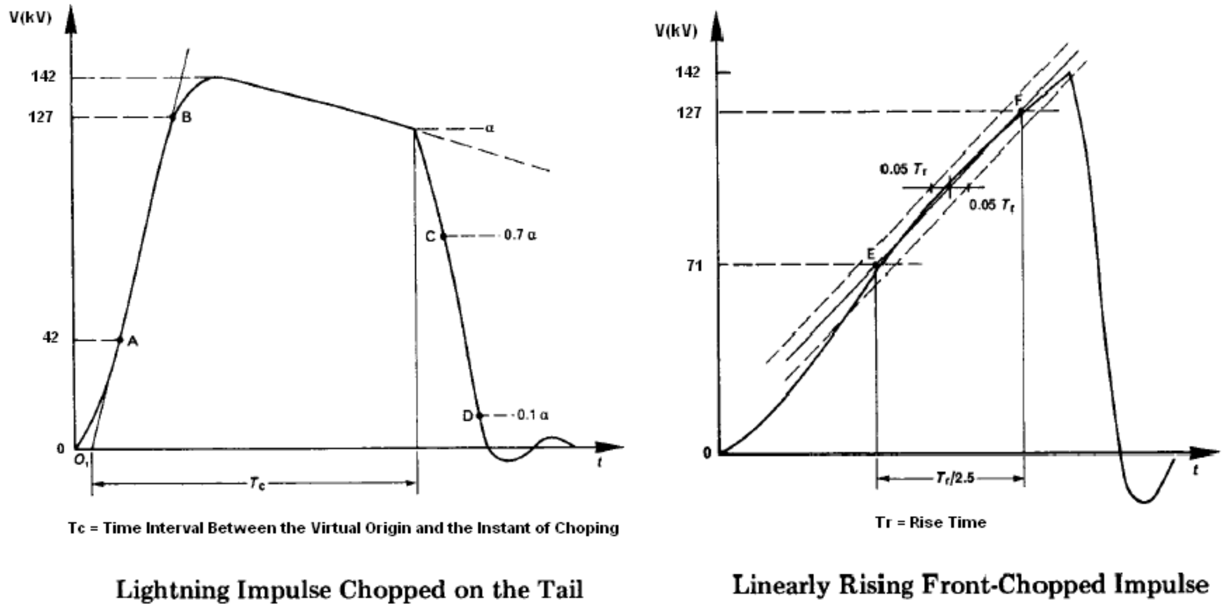


Figure 5-4 Waveform for Chopped Wave Impulse Test

The chopped wave shall have the following limits:

a) The virtual front time, based on the rated chopped wave test voltage, shall be equal to or less than 1.2 µs.
b) The peak voltage shall be equal to or greater than the rated chopped wave test voltage.
c) The time to the point of chop on the tail of the wave shall be no less than 2 µs. If the capacitance of a test sample is too high for test equipment to be able to produce a virtual front time as short as 1.2 µs, while maintaining the peak value, the most rapid rise obtainable may be used, subject to agreement between the user and the manufacturer.

NOTE—Flashovers external to the SSCL at the specified chop times, or longer, do not constitute failure

to pass the test

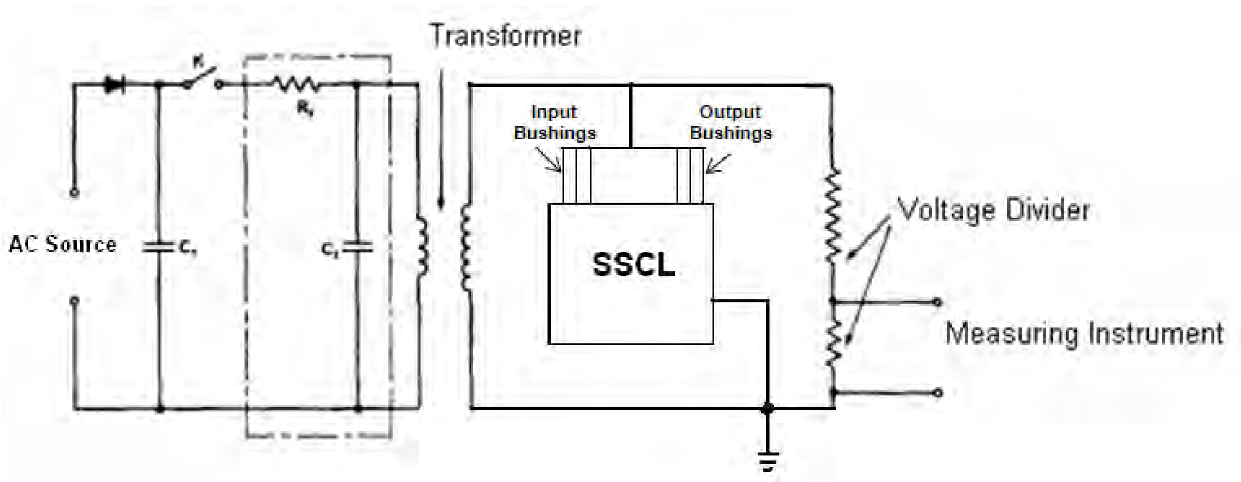


Figure 5-5 Test Schematic for Chopped Wave Impulse Test

5.2.1.6 Partial Discharge Test

Apparent internal partial discharges (apparent charge) shall be measured and reported in units of picocoulombs (pC). A partial discharge meter shall be used to measure the apparent charge generated by any internal partial discharges. The partial discharge detector, based on IEEE Std C57.113-1991, is used to measure the partial discharge levels at the terminals. General principles and circuits are described in IEEE Std 454-1973 [B6] and in IEEE Std C57.113-1991.

5.2.1.7 Insulation Power Factor Measurement

The voltage to be applied for measuring insulation power factor shall not exceed half of the low-frequency test voltage given in Table 5 of IEEE Std C57.12.00-2006 or 10 000 V, whichever is lower.

5.2.1.8 Insulation Resistance Measurement

A Megohmeter with nominal voltage of 500V will be used to measure insulation resistance.

5.2.2 Current Limiting Test

Objective: The current-limiting test of the SSCL is to demonstrate the current-limiting performance and the related capabilities of the SSCL.

5.2.2.1 Test conditions

5.2.2.1.1 Power factor

For current-limiting tests, the power factor of the testing circuits shall not exceed 5.9% lagging, equivalent to X/R = 17 at 60 Hz or 7.1% lagging equivalent to X/R = 14 at 50 Hz.

5.2.2.1.2 Frequency of test circuit

Tests demonstrating current-limiting capabilities shall be made at rated power frequency.

5.2.2.1.3 Current asymmetry

Current-limiting tests are required with both symmetrical and asymmetrical currents. Any current-limiting test in which the asymmetry of the current is less than 20% is considered a symmetrical test. Figure 5.1 shows the asymmetric fault current required to test the SSCL.

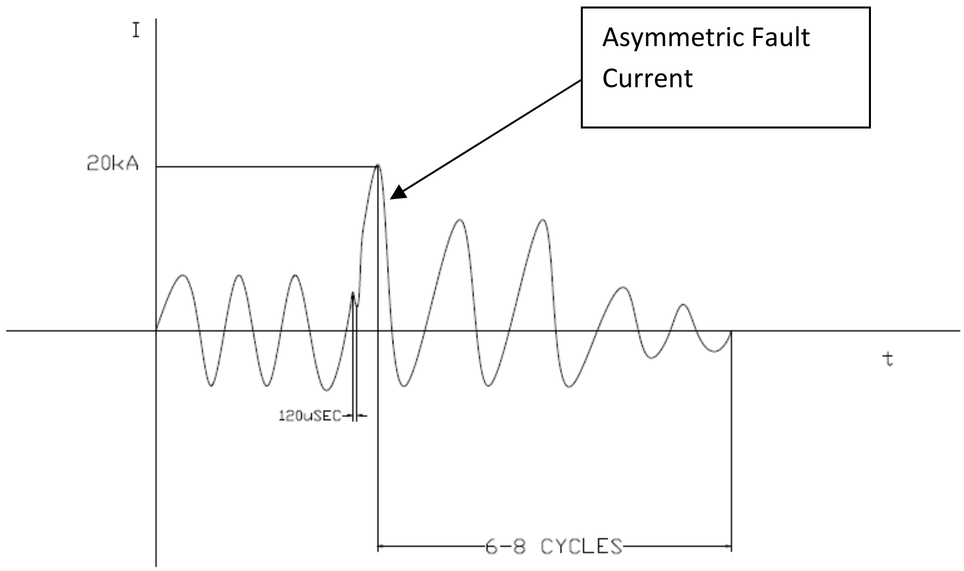


Figure 5-6 Asymmetric Fault Current

5.2.2.1.4 Obtaining the most severe switching conditions

To demonstrate the required current limiting capability of a SSCL, it is necessary to show that the SSCL is capable of meeting the requirements for the rated fault current. It must be shown that the SSCL is capable of limiting the rated current. Figure

5.2.3 Efficiency Test

Objective: The objective of this test is to measure the losses of the SSCL at various loads.

Test Schematic: Figure shows the proposed test schematic for the efficiency test.

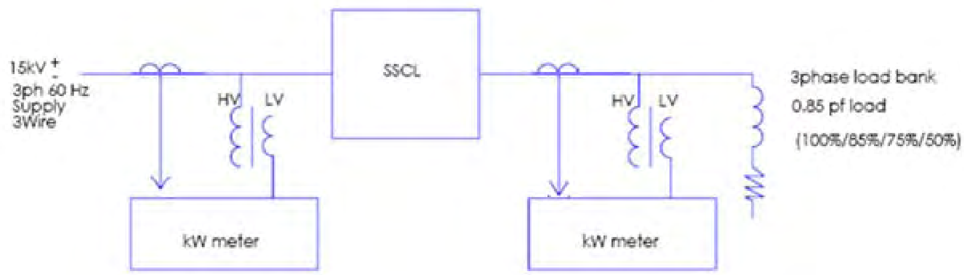


Figure 5-7 Efficiency Test Schematic

Test Description: A three phase, 0.85 power factor, load bank with 100%/ 85%/ 75%/ 50% taps will be connected to the load side of the SSCL. Readings will be taken using Voltage and current sensors at both ends of the SSCL as shown in the figure 5.2.

5.2.4 Continuous Current-carrying tests

Continuous current-carrying tests demonstrate that the SSCL can carry its rated continuous current, at its rated power frequency, without exceeding any of the temperature limitations.

5.2.4.1 Test conditions

a) The ambient temperature shall be between 10° C and 50° C, so that no correction factors need to be applied.
b) SSCL`s if normally equipped with current transformers shall be tested with transformers in place and connected to carry rated secondary current.
c) Tests demonstrating current carrying ability shall be done at voltage necessary to get rated continuous current.
d) Tests demonstrating current carrying ability shall be made at rated power frequency except that where tests are performed at 60 Hz they shall be considered to be valid for the same current rating with 50 Hz rated power frequency.
e) SSCL shall be tested with cables or buses of a size corresponding to the SSCL current rating connected to the SSCL terminals by means of typical terminal connectors of corresponding rating.

5.2.4.2 How tests shall be made

a) Three-phase SSCL`s shall be tested on a three-phase or single-phase basis.

b) Where there is no possibility of magnetic influence, but there may be thermal influence from other phases of the SSCL, tests may be made with single-phase current passed through the three poles in series.

5.2.4.3 Duration of continuous current tests

The continuous current test shall be continued for a period of time such that the temperature rise of any monitored point in the assembly has not changed by more than 1.0 °C as indicated by three successive readings at 30 min intervals.

The equipment is considered to have passed the test if the established temperature limits specified in IEEE Std C37.04-1999 have not been exceeded in any of the last three readings.

5.2.4.4 How temperatures are measured

Temperatures shall be measured by any of the following methods (see IEEE Std 119 Aug.1950):

a) Thermocouple
b) Thermometer (allowed method only for ambient temperature measurements; not acceptable for temperature measurement of current carrying components)

The measuring device shall be located at a point where measurement of the hottest accessible spot can be made. Measurements shall be made at junction points of insulation and conducting parts to prevent exceeding temperature limits of the insulation.

5.2.4.5 How ambient temperature is determined

The ambient temperature is the average temperature of the surrounding air, external to the circuit breaker enclosures.

The ambient temperature shall be between 10°C and 50°C, so that no correction factors need be applied. The ambient temperature shall be determined by taking the average of the readings of three measurements that are made at locations unaffected by drafts approximately 300 mm (12 in), away, horizontally, from the projected periphery of the SSCL or enclosure, and approximately in line, vertically, as follows:

a) One approximately 300 mm (12 in) above the SSCL (including bushings).
b) One approximately 300 mm (12 in) below the SSCL.
c) One approximately midway between the above two positions.

To avoid errors that are due to the time lag between the temperature of large apparatus and the variations in the ambient temperature, the measuring device used for determining the ambient temperature shall be immersed in a suitable liquid, such as oil, which is contained in a suitable heavy metal cup.

5.2.5 Audible Sound Test

The audible sound will be measured using microphones at Alion/R&B Laboratory.

5.2.6 Radio Influence Voltage (RIV) Test

The conducted radio noise will be measured using a test circuit in accordance with NEMA and ANSI C36.2 specifications.

5.2.7 Electrical Noise/EMI Test

Electrical Noise/Electromagnetic interference will be measured at Alion/R&B Laboratory.

5.3 Testing at SCE

5.3.1 SSCL Interfaces

SSCL will be equipped with the following sensors

- Dial Type Thermometer
- Pressure Gauge
- Current Transformer
- SEL HMI – RS232 and Ethernet ports for system voltage and current monitoring

5.3.2 Acceptance Test at SCE

These tests will be performed by SCE at their Westminster facility in accordance with their test procedures.

5.3.2.1 Winding Resistance Test

5.3.2.2 Winding Impedance Measurement

5.3.2.3 Turn to Turn Test

5.3.2.4 Total Loss Measurement Test

5.3.2.5 Voltage-freq Withstand Test

5.3.2.6 RIV Test

5.3.2.7 BIL Test

5.3.2.8 Chopped-wave Test

5.3.2.9 Audible Noise Test

5.3.2.10 Partial Discharge Test

5.3.2.11 Insulation Resistance Measurement

5.3.2.12 Fault current Limiting Test followed by Normal Operation Test

5.3.2 Field Evaluation Testing at Shandin Sub-station

5.3.2.1 Pre-connection

5.3.2.1.1 External Inspection

All SSCLs will be carefully tested at the manufacturing unit and will be in good condition before the shipment is made. Once received at site an external inspection of the SSCL tank and fittings will be done which will include the following points:

1. Is there any indication of external damage?
2. Is the paint finish damaged?
3. Are the attached fittings loose or damaged?
4. Is there evidence of fluid leakage on or around the tank coolers?
5. Are any of the bushings broken or damaged?
6. Is there any visible damage to the parts or packaging which shipped separately from the SSCL?

5.3.2.1.2 Tank Pressure

The tank pressure may be positive or negative when received, depending on liquid temperature. In some cases, the vacuum pressure gauge may read zero, which could indicate a tank leak. In such cases, pressure test of the tank shall be done.

5.3.2.1.3 Winding Resistance Measurement

This test will be performed by SCE in accordance with their test procedures.

5.3.2.1.4 Winding Impedance Measurement

This test will be performed by SCE in accordance with their test procedures.

5.3.2.1.5 Insulation Power factor Test

This test will be performed by SCE in accordance with their test procedures.

5.3.2.1.6 Insulation Resistance

This test will be performed by SCE in accordance with their test procedures.

5.3.2.2 Field evaluation testing

5.3.2.2.1 Operational Test (Steady State & Transient)

Objective: The objective of this test is to monitor the SSCL performance under Steady-State condition of the system in which the SSCL is connected.

Test Schematic: Figure shows the proposed test schematic for the operational test

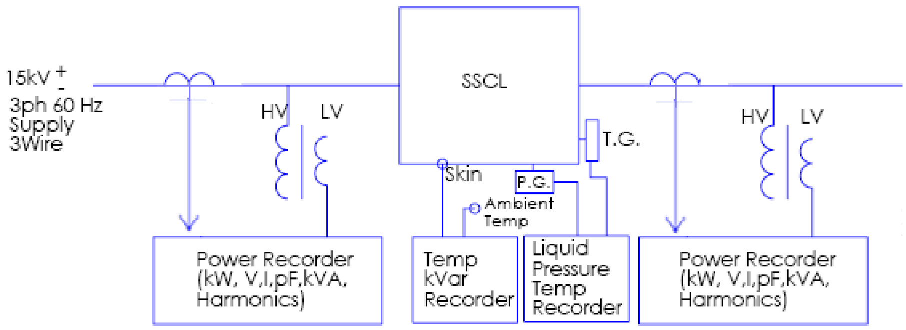


Figure 5-8 Operational Test Schematic

Test Description: The SSCL will be connected to the 15kV line and load side. Readings will be taken using voltage and current sensors at both ends of the SSCL as shown in the figure. Power, voltage current and power factor will be monitored and recorded with the help of the power monitoring/ recorder. Temperature of the surface of the tank and the cooling liquid will be measured and recorded with the help of the temperature sensors and recorder as shown in the test schematic. Cooling liquid pressure will also be monitored with the help of a pressure gauge.

6 SCHEDULE

Test #	Description	Month-1	Month-2	Month-3	Month-4	Month-5	Month-6	Month-7	Month-8	Month-9	Month-10	Month-11	Month-12
Design verification Tests													
	Dielectric tests												
1	Power Freq. Voltage Withstand test												
2	Basic Impulse Voltage Withstand test												
3	Chopped wave Voltage Withstand test												
4	**Current-limiting tests**												
5	**Elect. Efficiency tests**												
6	**Continuous current capabolity Tests**												
7	**Dielectric/ Power Freq. Voltage Withstand test**												
	Refurbish & ship Unit to SCE												
Field evaluation Tests													
8	**Pre-installation tests**												
9	**Field testing**												

A TABLE OF TESTS

Name of Test	Description	Location of Test
Component level:		
CLR – Inductance/Impedance Meas.	144 µH	KEMA Power Labs
CLR – Turn-to-turn Voltage Meas.		KEMA Power Labs
CLR – Let-through Current	9000A rms sym. for 0.5sec	KEMA Power Labs
Aux Power Supply Transformer	Insulation, loading & cont. operation test	SPCO/ KEMA Power Labs
Aux Power Supply Inverter	Insulation, loading & cont. operation test	SPCO/ KEMA Power Labs
Current Interruption Test (Building Block)	At 5000A peak from 23kA rms sym. Available fault current	KEMA Power Labs
Continuous Current/Temp. rise Test (Building Block)	1200A rms at low voltage	KEMA Power Labs
System level At SPCO:		
Insulation resistance (Megger) test	13000 M-ohm at 3000V DC	KEMA Power Labs
Current Limiting Test	Limiting to 9kA rms sym from available 23kA rms sym	KEMA Power Labs
Efficiency Test	@ 25%, 50%, 75%, 90%, 100% Load	KEMA Power Labs
Audible Noise Test	@ 25%, 50%, 75%, 90%, 100% Load	KEMA Power Labs
Nominal-freq voltage withstand test	50kV rms for 1minute	KEMA Power Labs
BIL Test	110kV	KEMA Power Labs
Chopped wave test	142 kV peak	KEMA Power Labs
Continuous Current/ Temp. rise Test	1200A rms at low voltage	KEMA Power Labs
BIL Test (repeat test after continuous current test)	110kV	KEMA Power Labs
Partial Discharge	Up to 15kV. 100 pC	KEMA Power Labs
RIV Test	TBD	R&B /Alion Lab
Electrical noise/EMI Test	TBD	R&B /Alion Lab

Acceptance test At SCE Lab:		
Winding resistance test		Westminster facility
Winding impedance test		Westminster facility
Turn to turn test		Westminster facility
Total loss measurement Test		Westminster facility
Voltage-freq withstand test	50kV rms for 1minute	Westminster facility
RIV Test	At 120% of Nominal Voltage	Westminster facility
BIL Test	110kV	Westminster facility
Chopped-wave	142kV peak	Westminster facility
Audible Noise Test		Westminster facility
Partial Discharge	19.5kV pre-stressed, 16.5kV , 100 pico-coulomb	Westminster facility
Insulation Measurement	at 10kV 13,000 mega-ohm	Westminster facility
Insulation power factor test		Westminster facility
Fault current limiting test followed by normal operation	23kA for 10 cycles	Westminster facility
System level At SCE Field:		
Winding resistance		Shandin Substation, CA
Winding impedance		Shandin Substation, CA
Insulation PF test		Shandin Substation, CA
Insulation resistance		Shandin Substation, CA
Operations test	Normal, Current-limiting	Shandin Substation, CA